



Cache-Coherent Shared Locking for Transactionally Consistent Updates in Near- Data Processing DBMS on Smart Storage

Arthur Bernhardt, Sajjad Tamimi, Florian Stock, Tobias Vinçon,
Andreas Koch, Ilia Petrov



Motivation

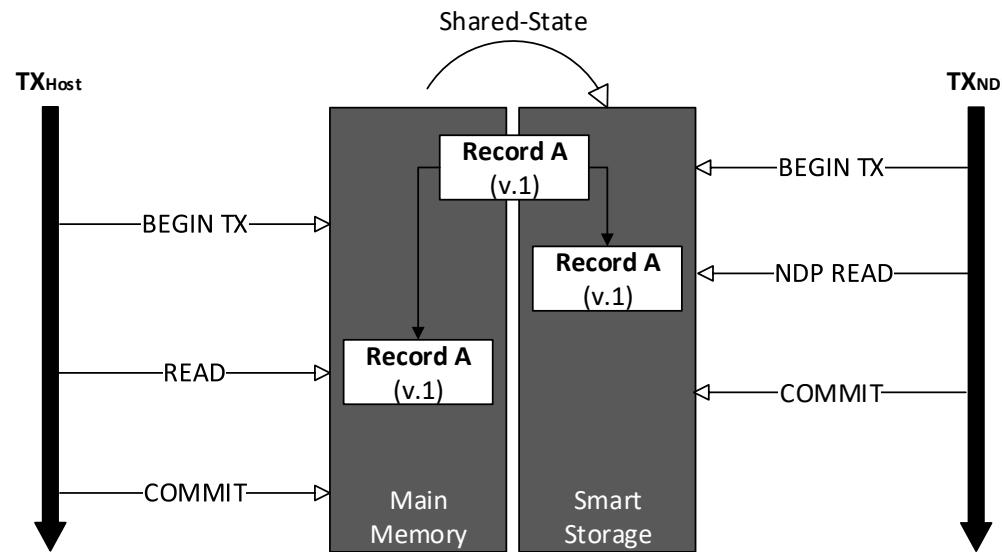


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Read-only NDP:

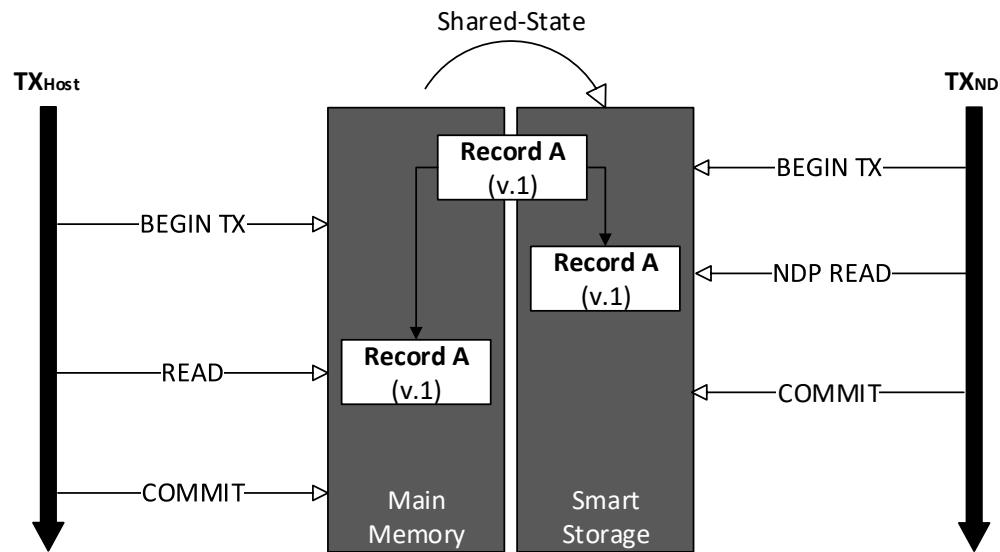


Motivation



Read-only NDP:

-> Snapshot-based, intervention-free NDP



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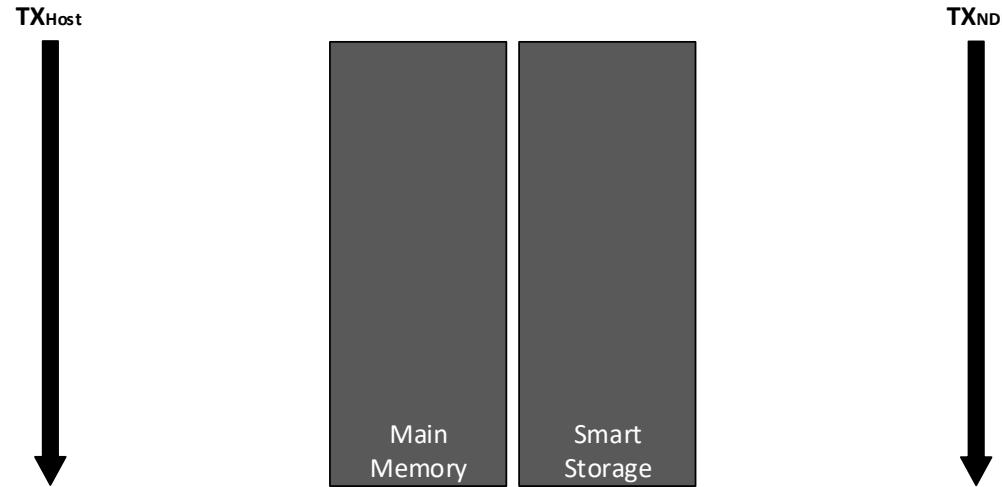


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Update NDP:



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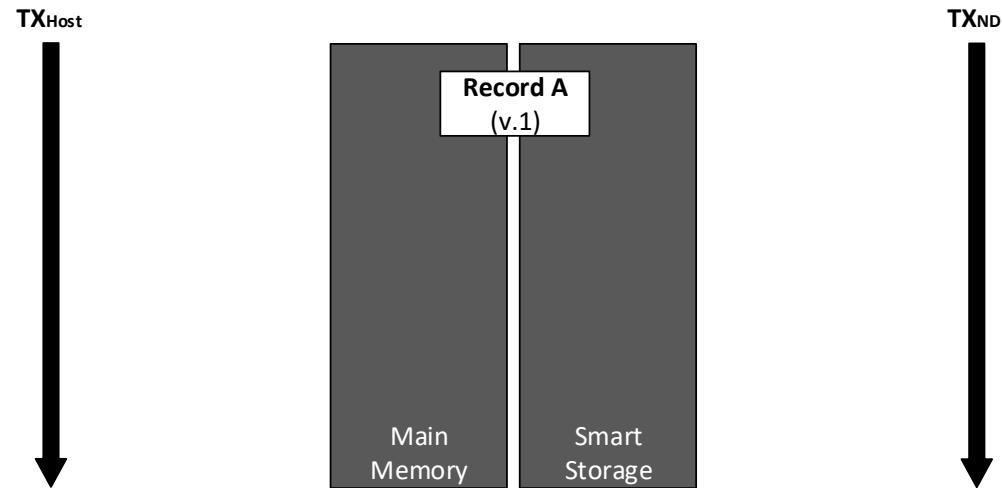


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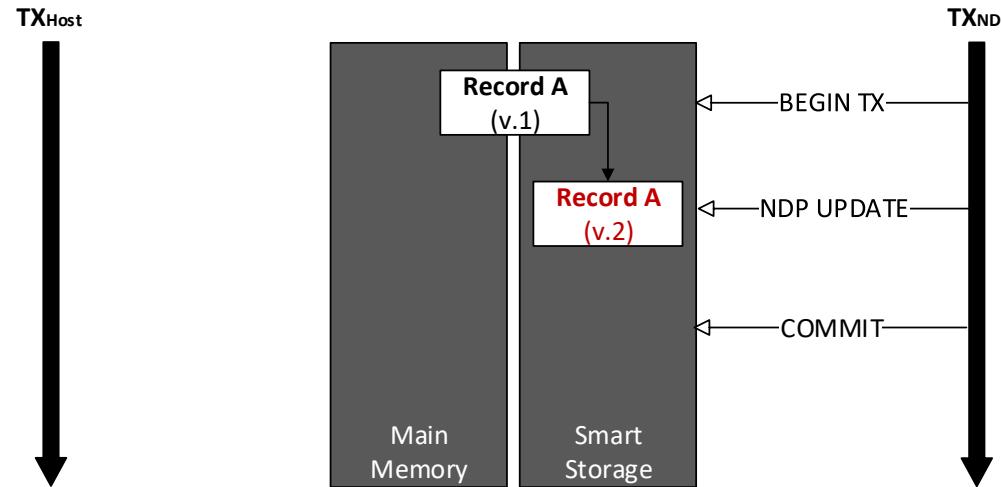


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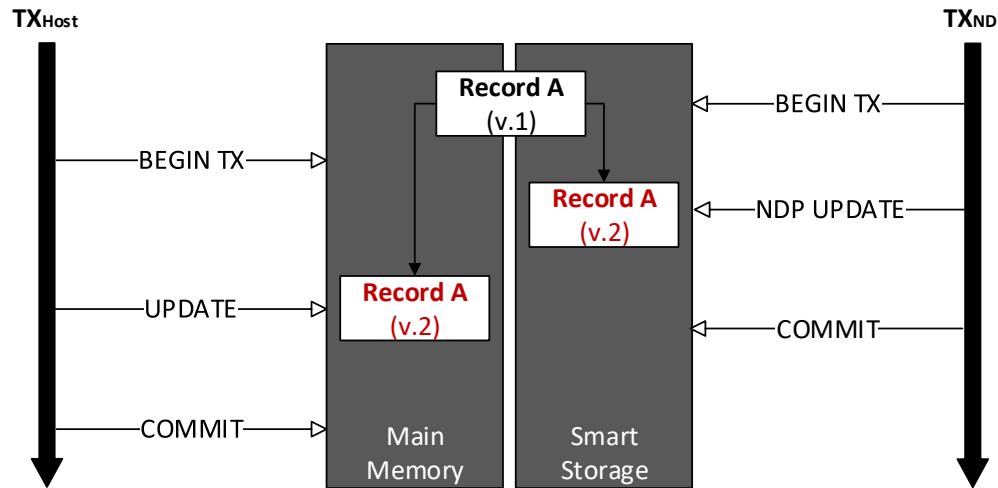


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Update NDP:

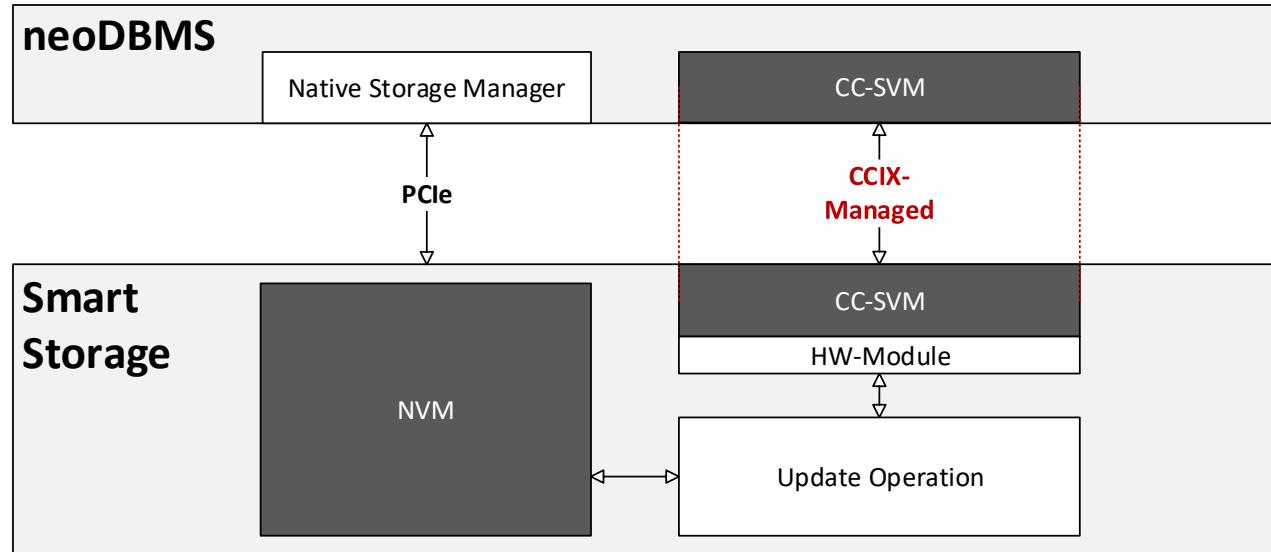
-> Synchronization problems



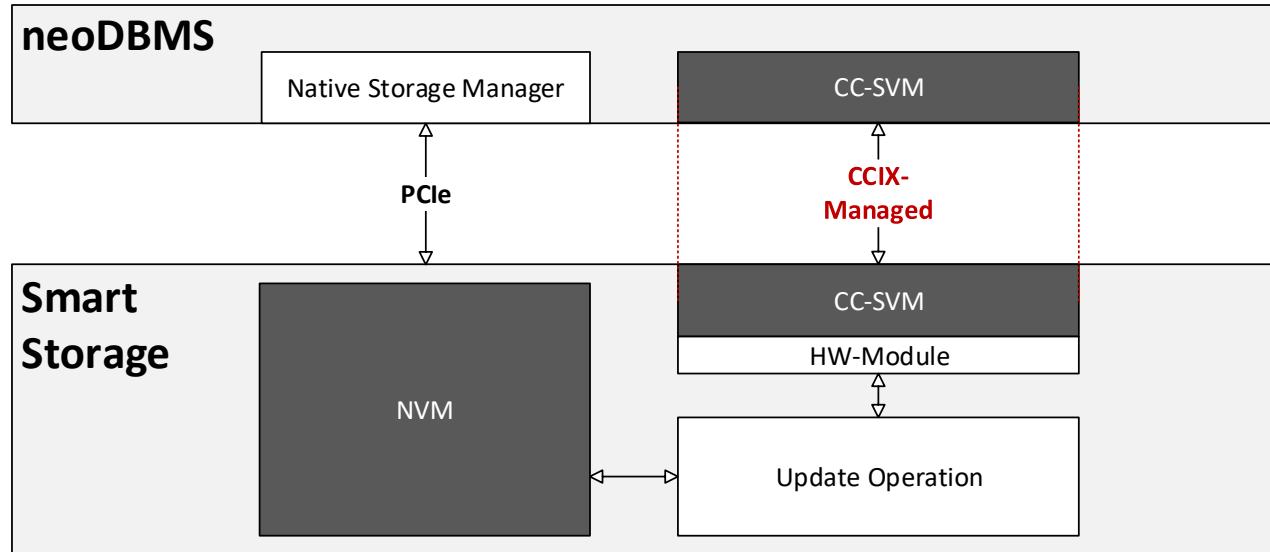
Multiple version branches cause unresolvable inconsistencies!



Goal: Enable efficient synchronization mechanisms between DBMS and Smart Storage for transactionally consistent updates in NDP-settings



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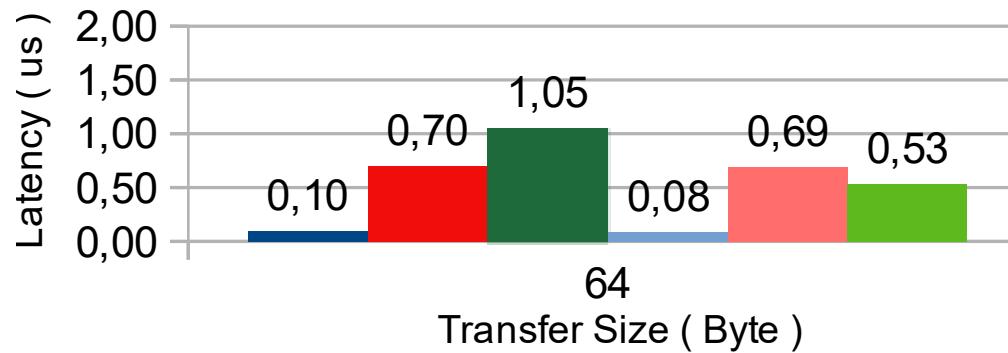
Synchronization requires cache coherence and low-latency transfers!



Cache-Coherent Interconnect for Accelerators (CCIX)

- Cache-coherent data sharing between devices
- High signaling rates 16-25 GT/s per link
- Address translation and cache coherence is automatically maintained
- Supports atomics like CAS

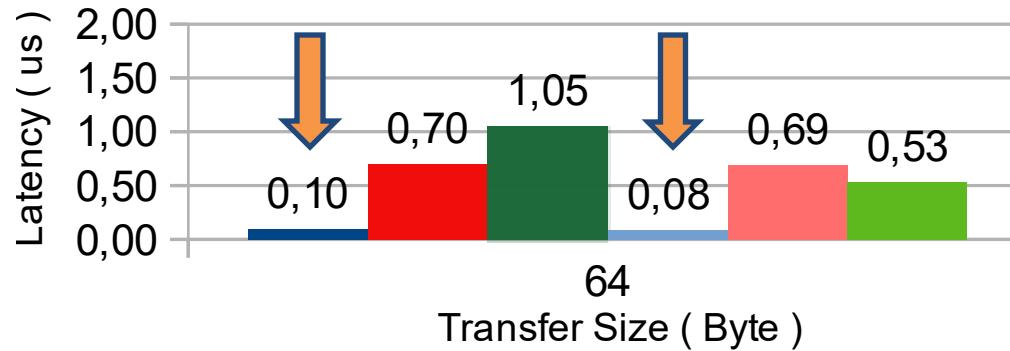
■ CCIX Read ■ CCIX Read (cache-miss) ■ PCIe Read
■ CCIX Write ■ CCIX Write (cache-miss) ■ PCIe Write



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CCIX provides excellent latencies for small granularity accesses!



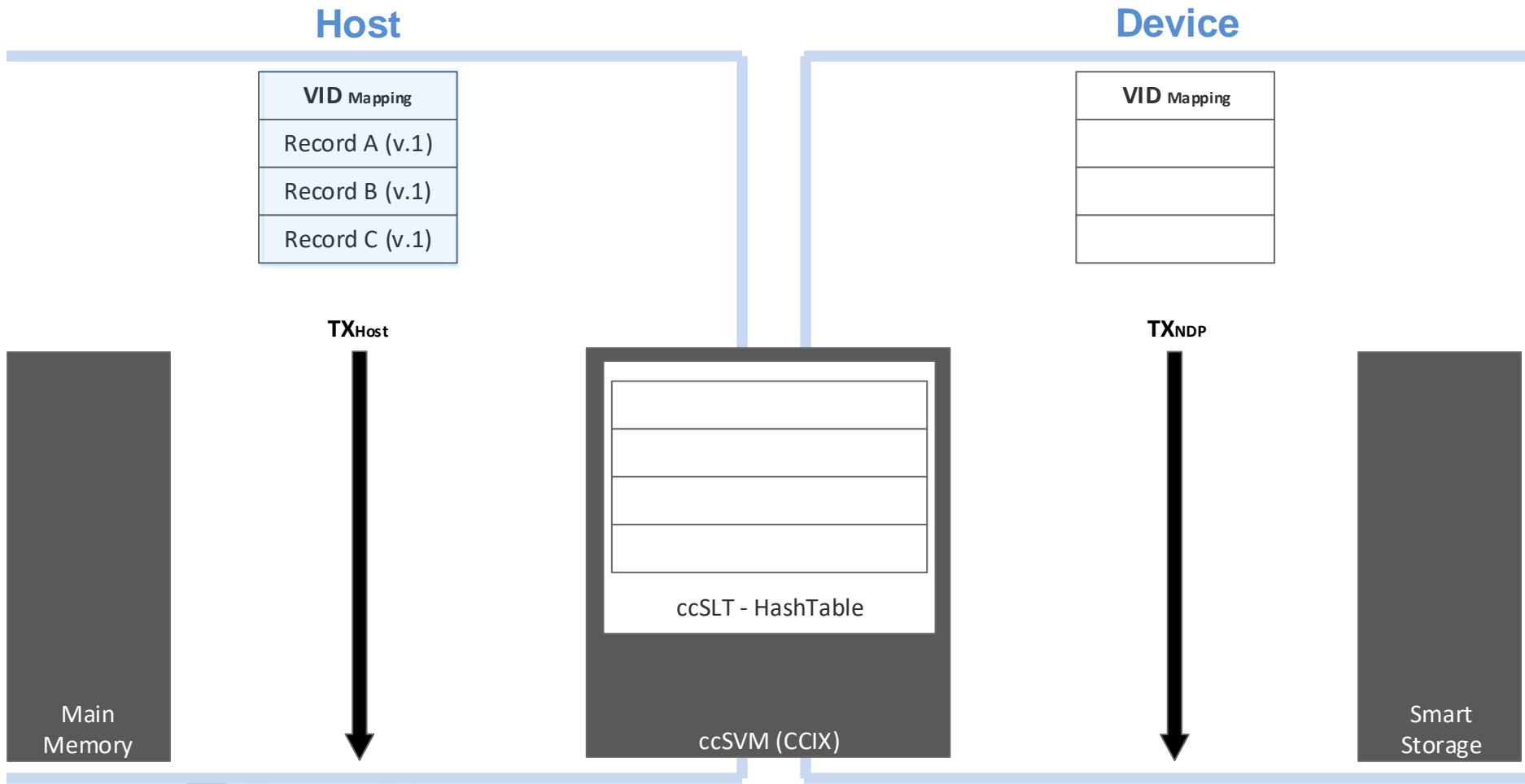
CC Shared Lock Table



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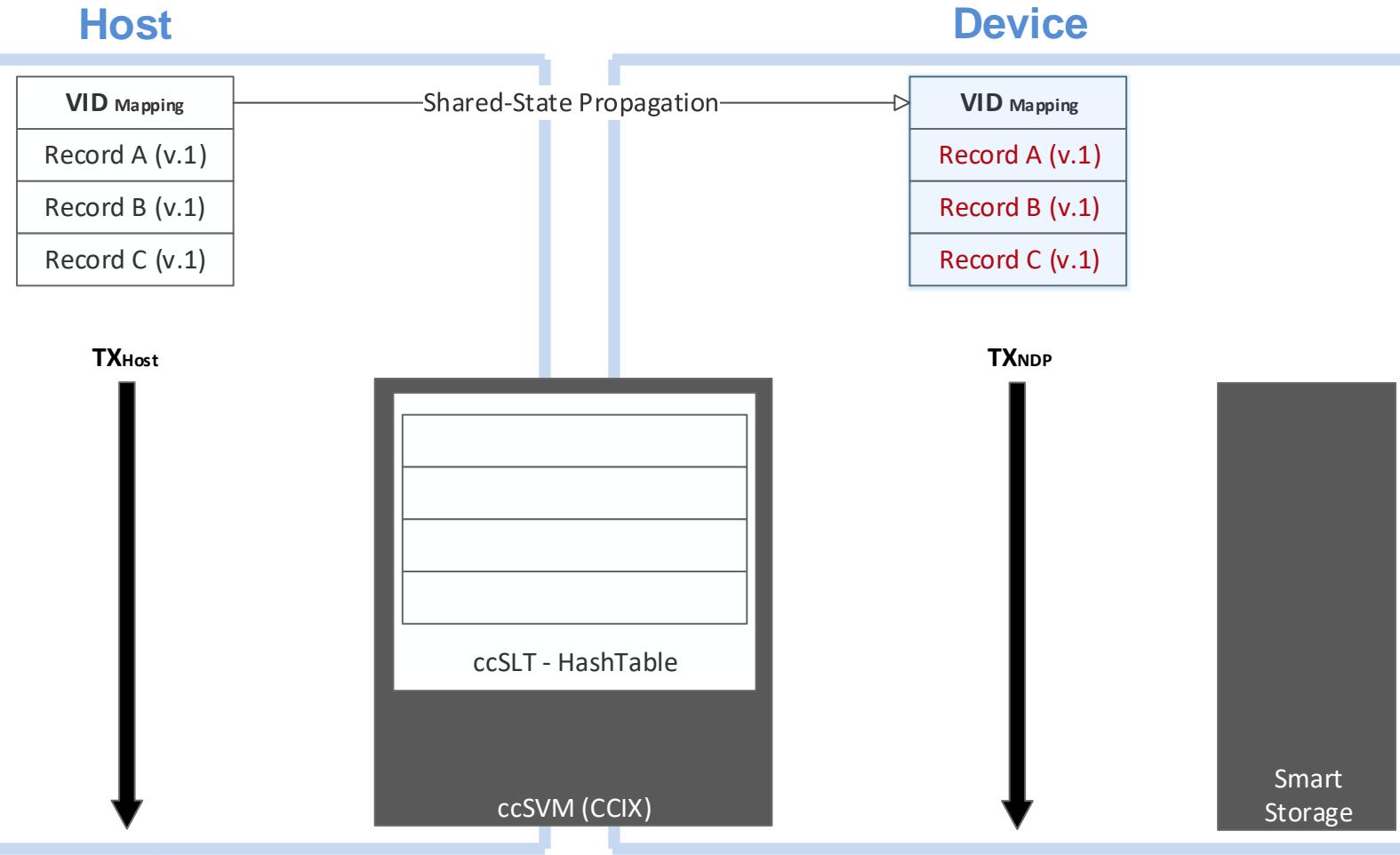
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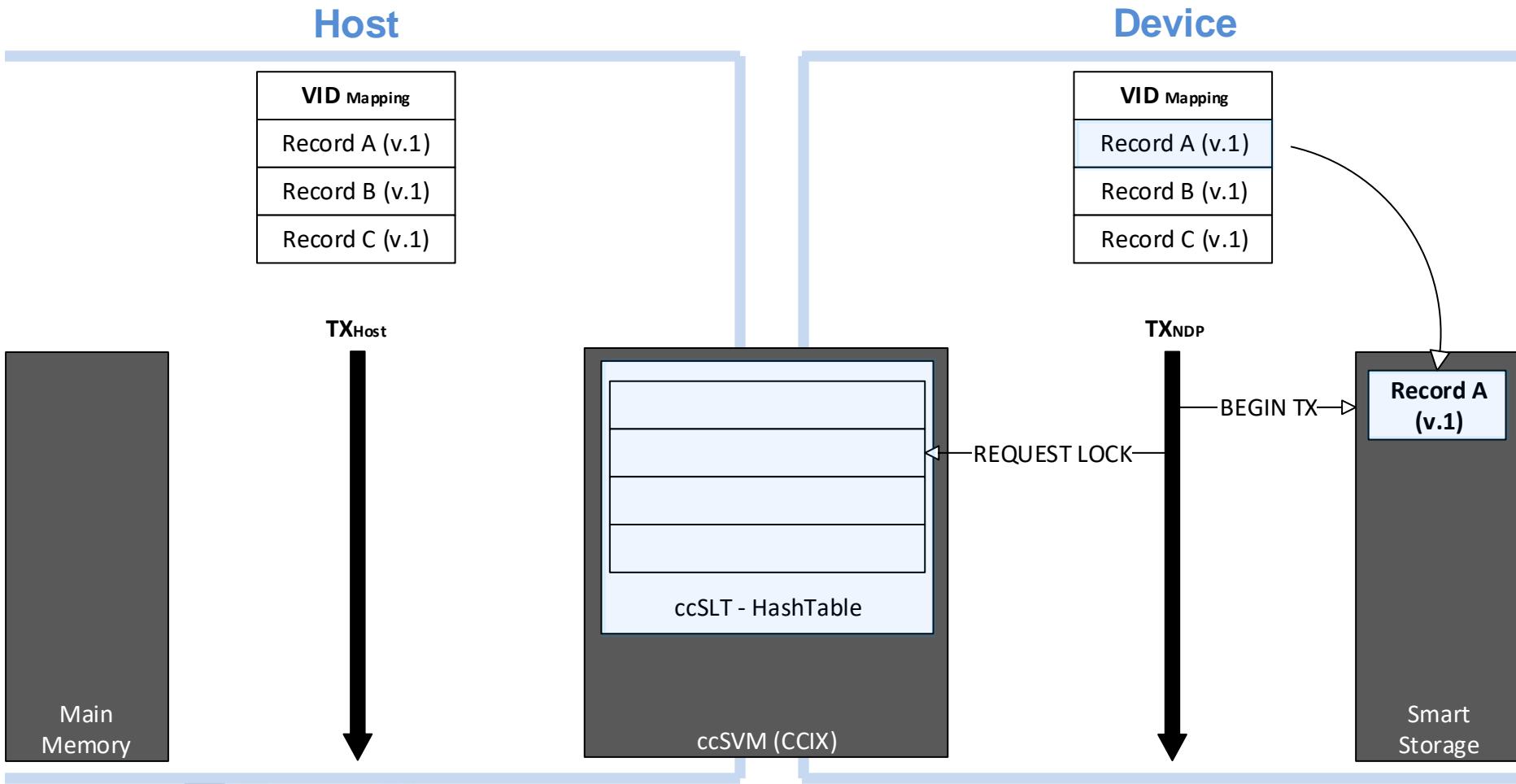
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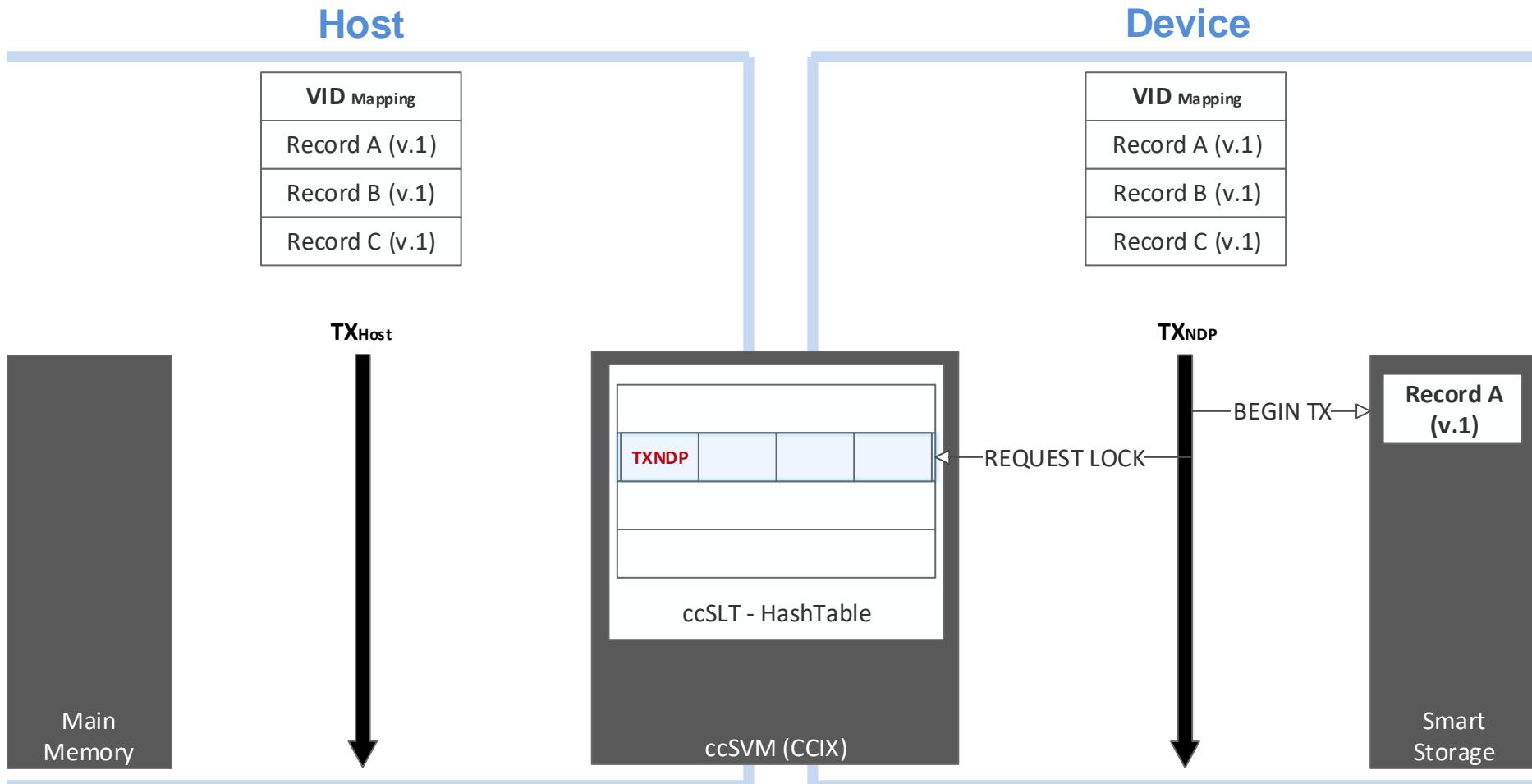
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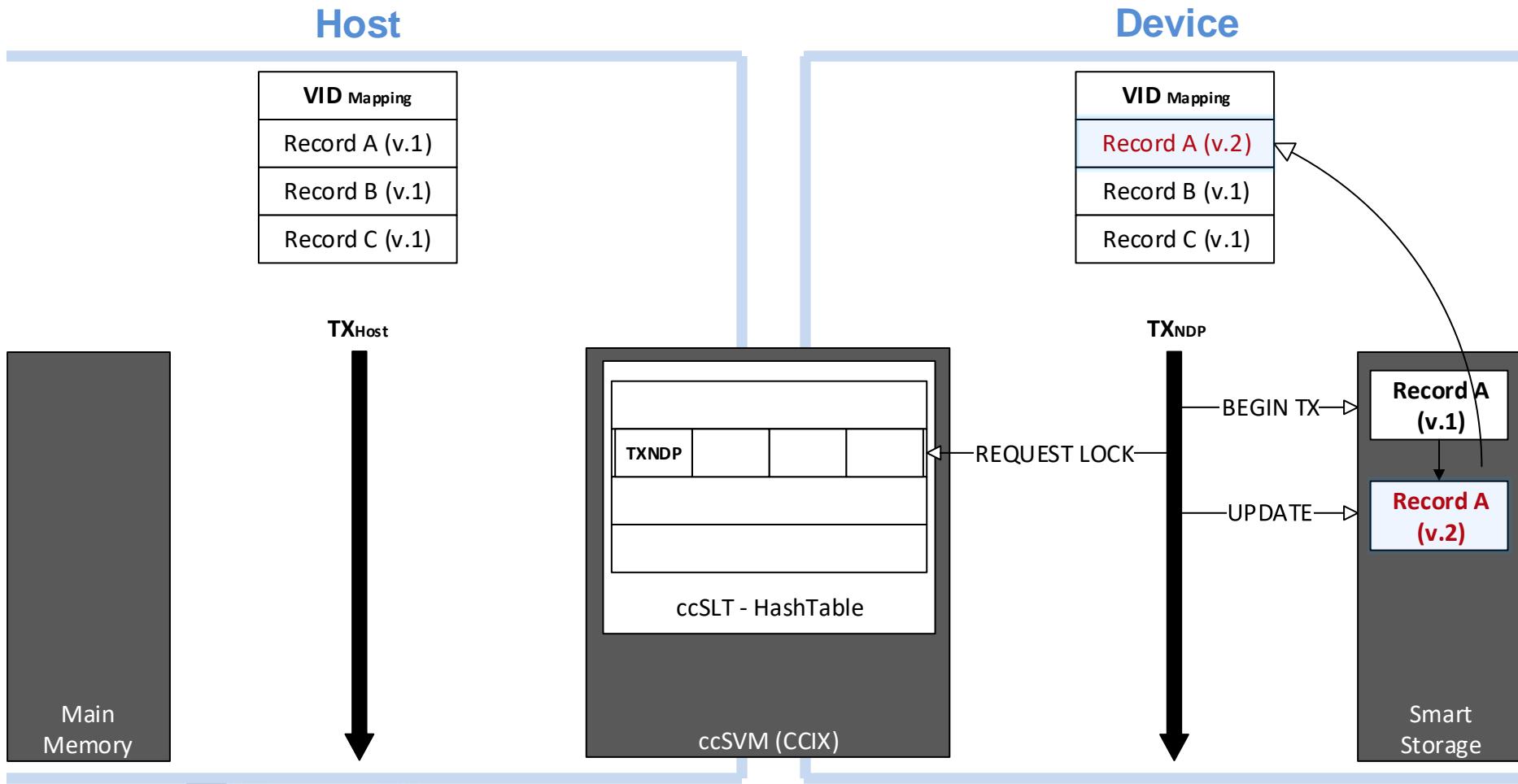
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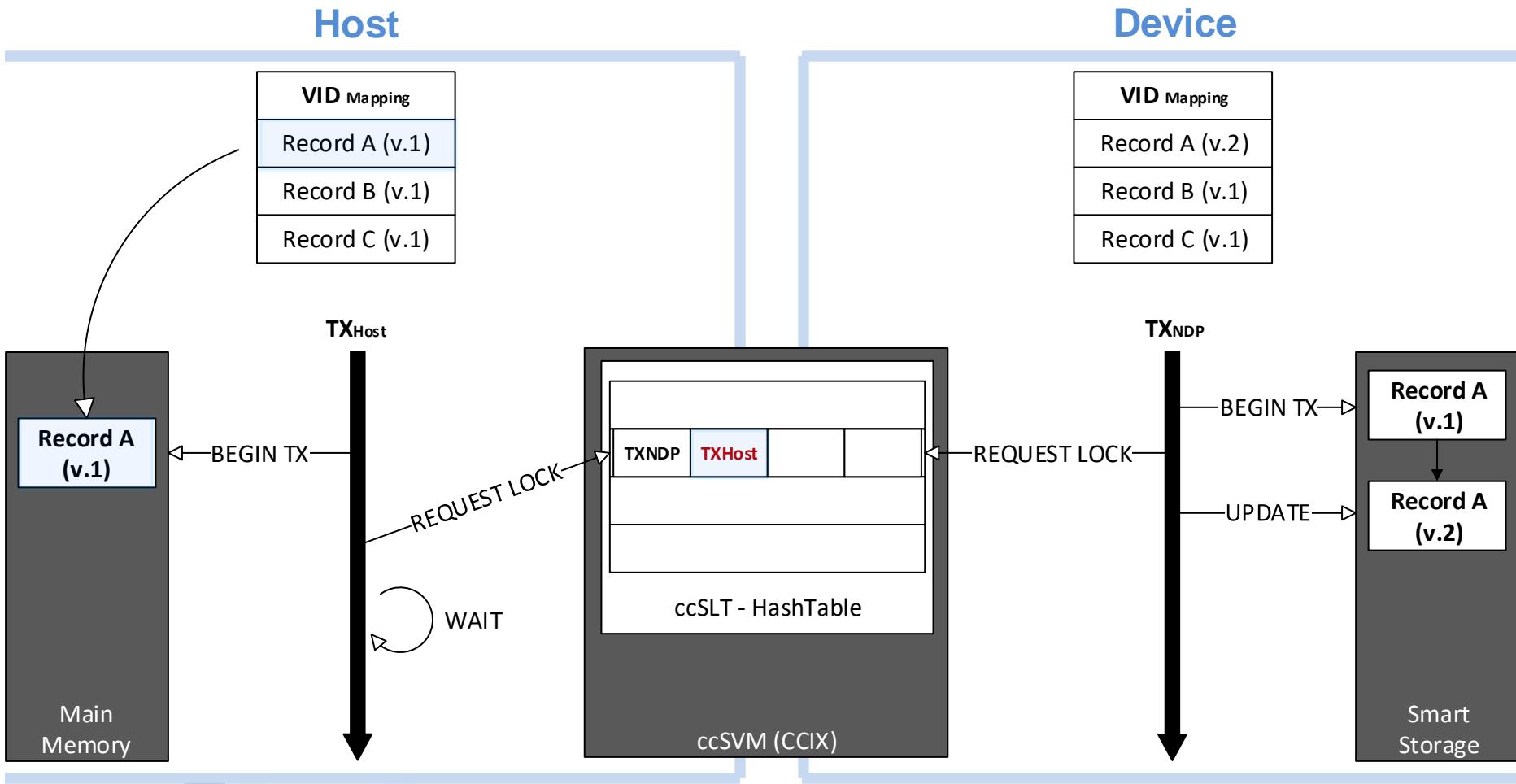
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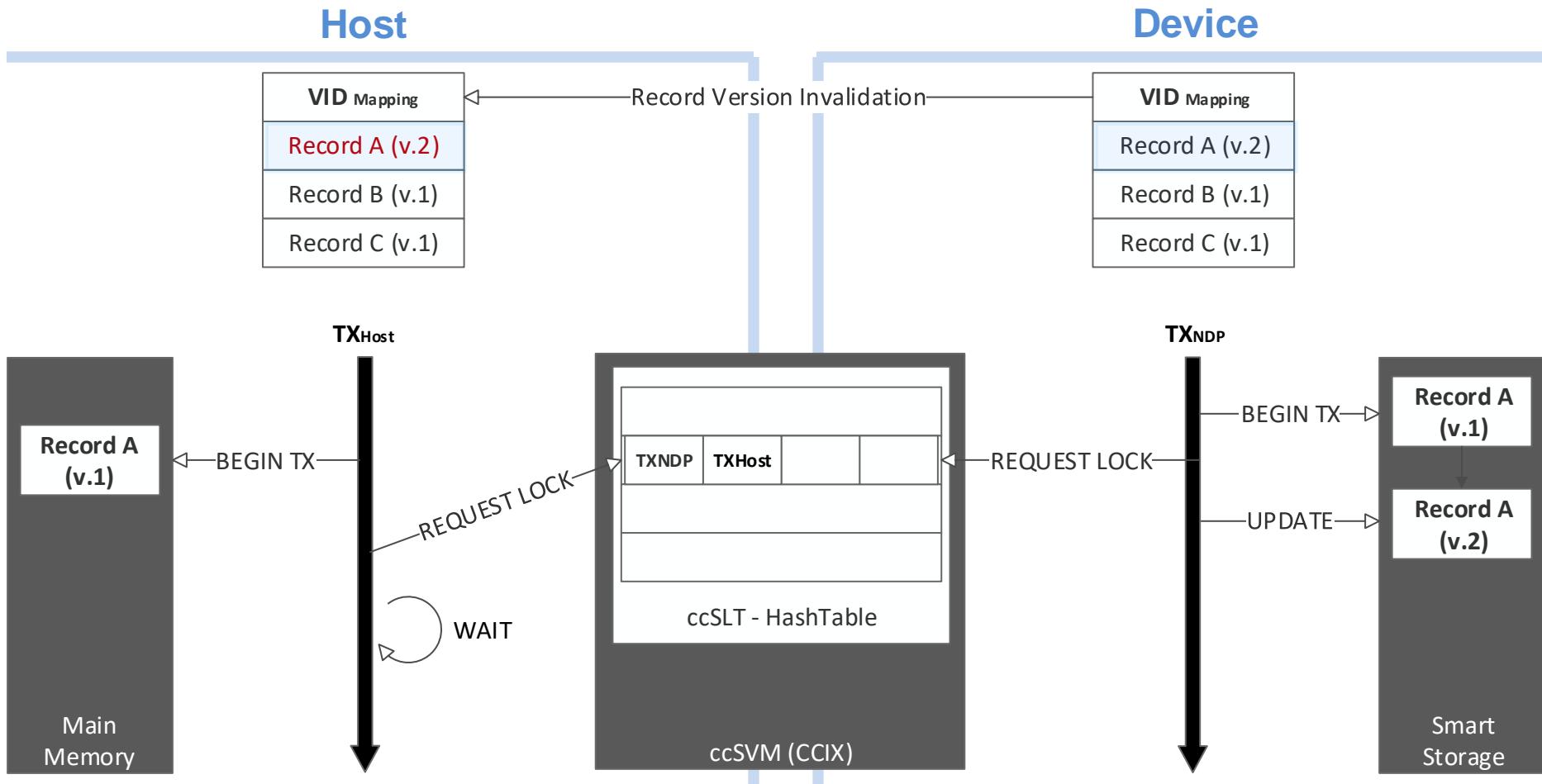
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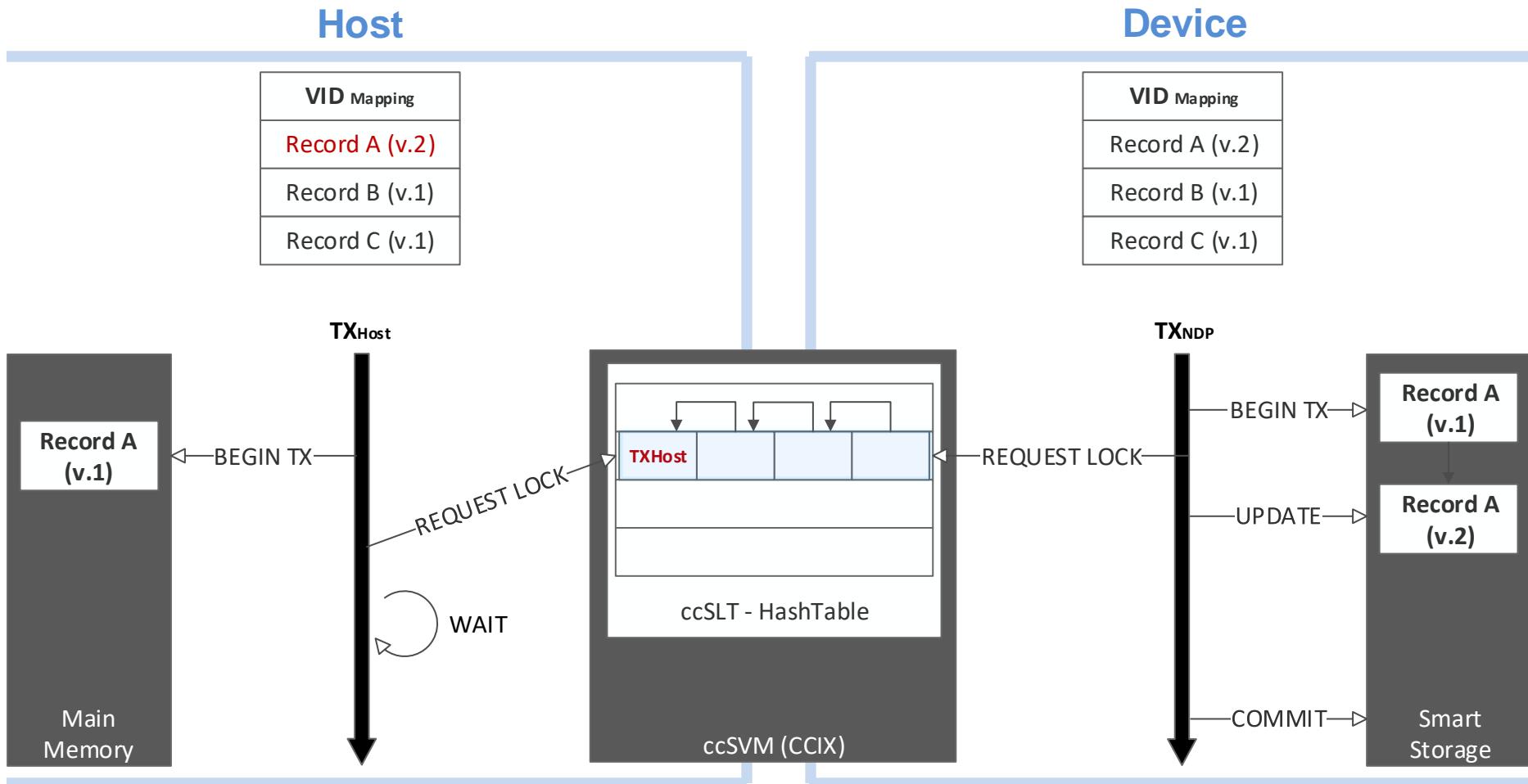
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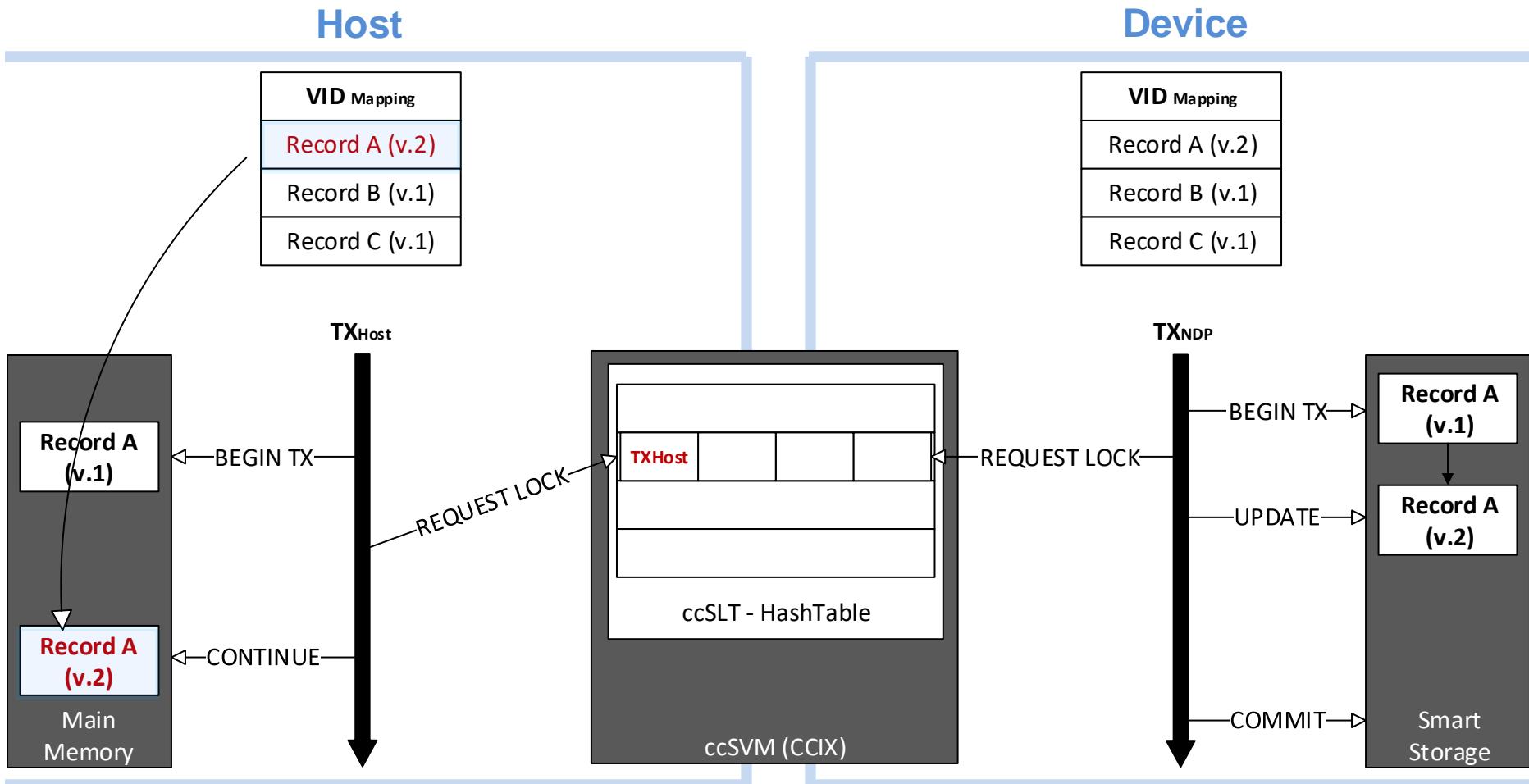
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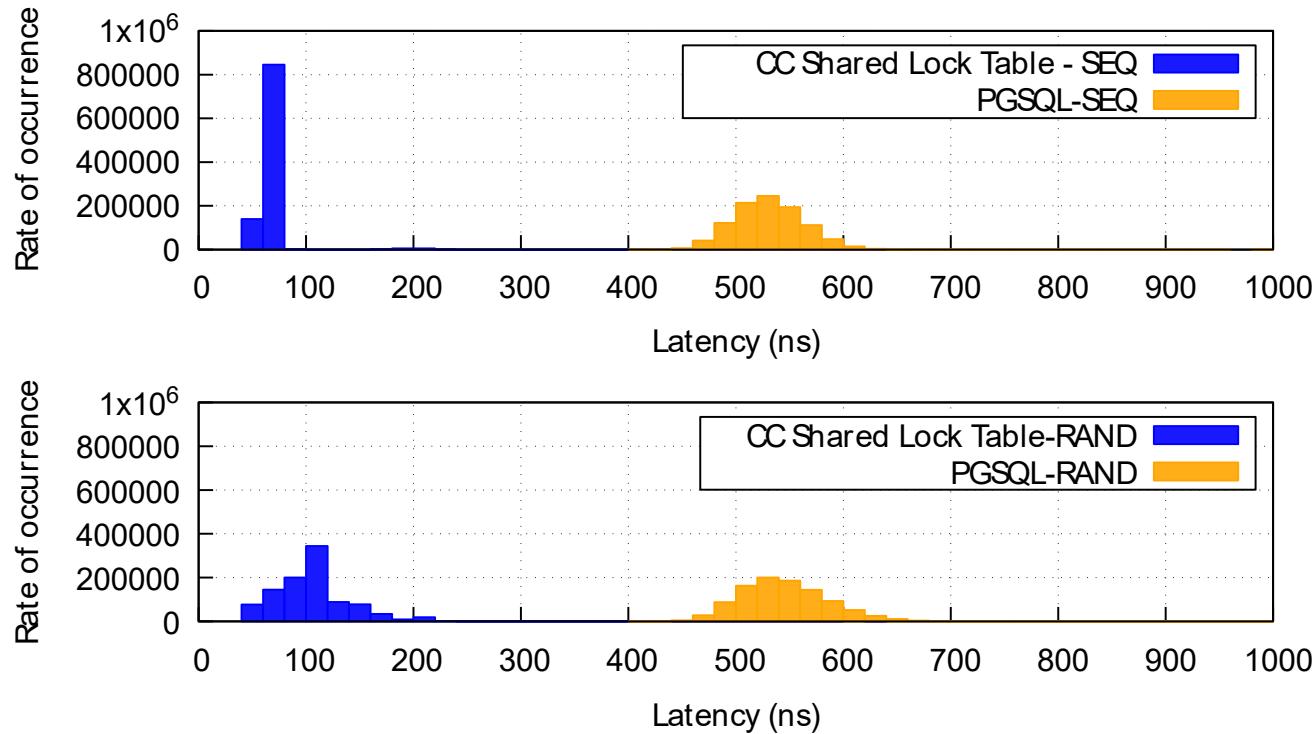
Experimental Evaluation



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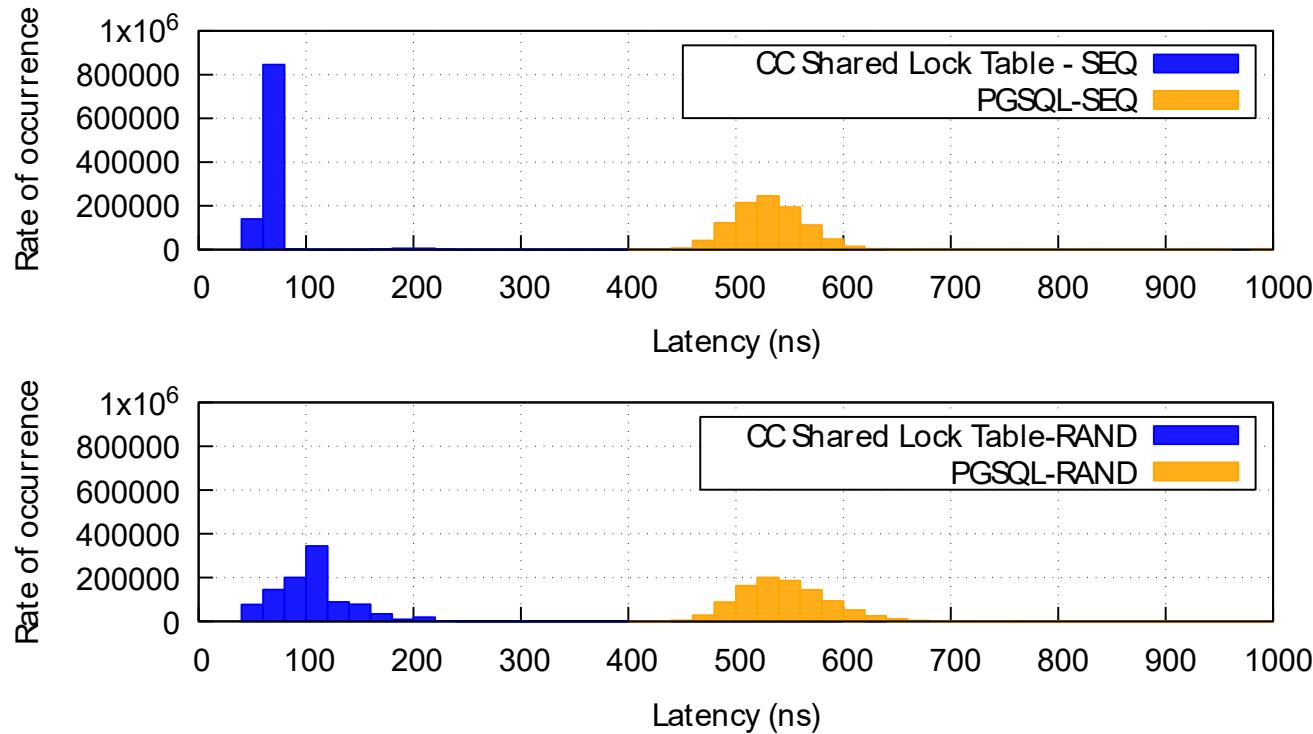
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Host and smart storage synchronization is enabled with very low overhead!





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„People who are really serious about
software should make their own hardware,,

Dr. Alan Kay, 2003 Turing Award Laureate

