Design-Space Exploration with Multi-Objective Resource-Aware Modulo Scheduling

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2: Imperial College London

4: KIT Karlsruhe Institute of Technology

Agenda

- ▶ **Introduction to high-level synthesis**
- □ Resource-aware modulo scheduling
- □ Exploration of trade-off solutions
- □ Experimental evaluation

FPGAs

- Field-Programmable Gate Arrays
  - semiconductor chips, ideal for energy-efficient, application-specific accelerators

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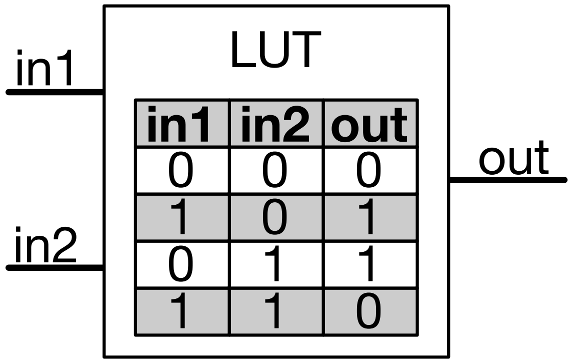
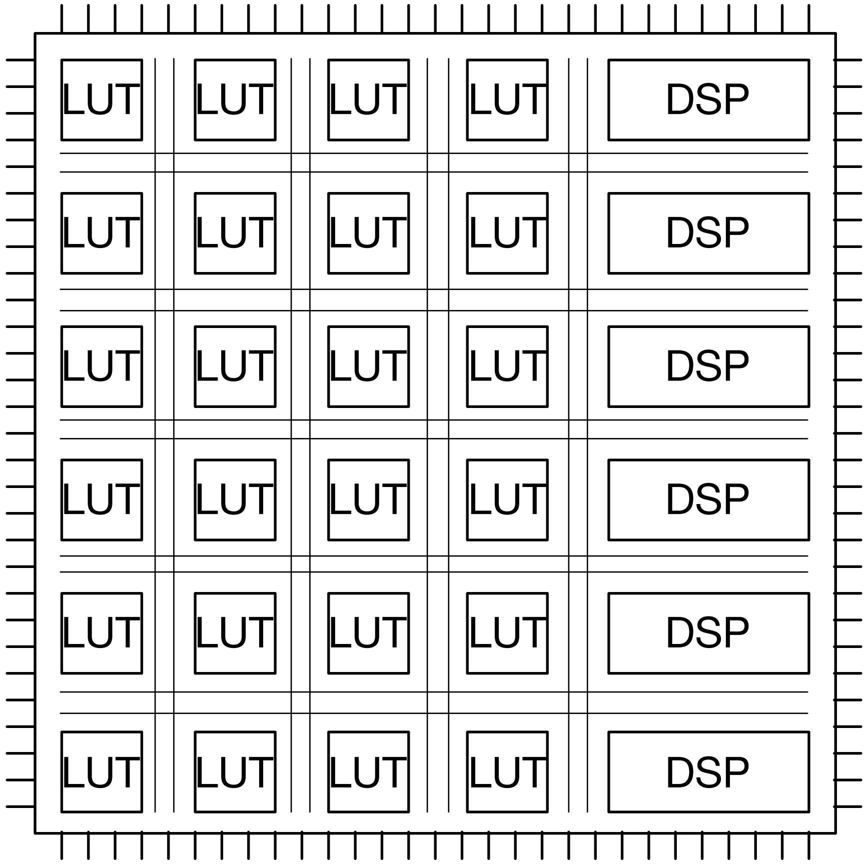
  - comprised of **resources**
    - look-up tables (LUT)
    - DSP blocks
    - …
    - programmable interconnect



in1	in2	out
0	0	0
1	0	1
0	1	1
1	1	0

out = in1 xor in2



LUT	LUT	LUT	LUT	DSP
LUT	LUT	LUT	LUT	DSP
LUT	LUT	LUT	LUT	DSP
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  - semiconductor chips, ideal for energy-efficient, application-specific accelerators
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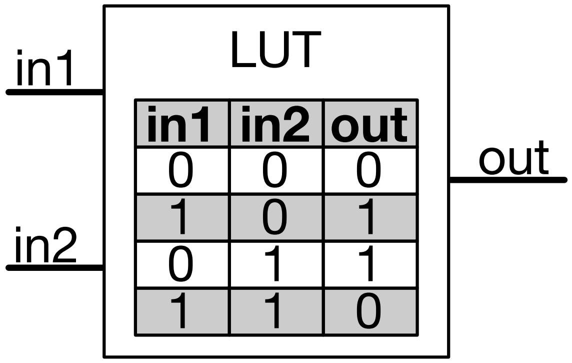
    - …
    - programmable interconnect
  - „programming“ FPGA
    = configuring and connecting resources



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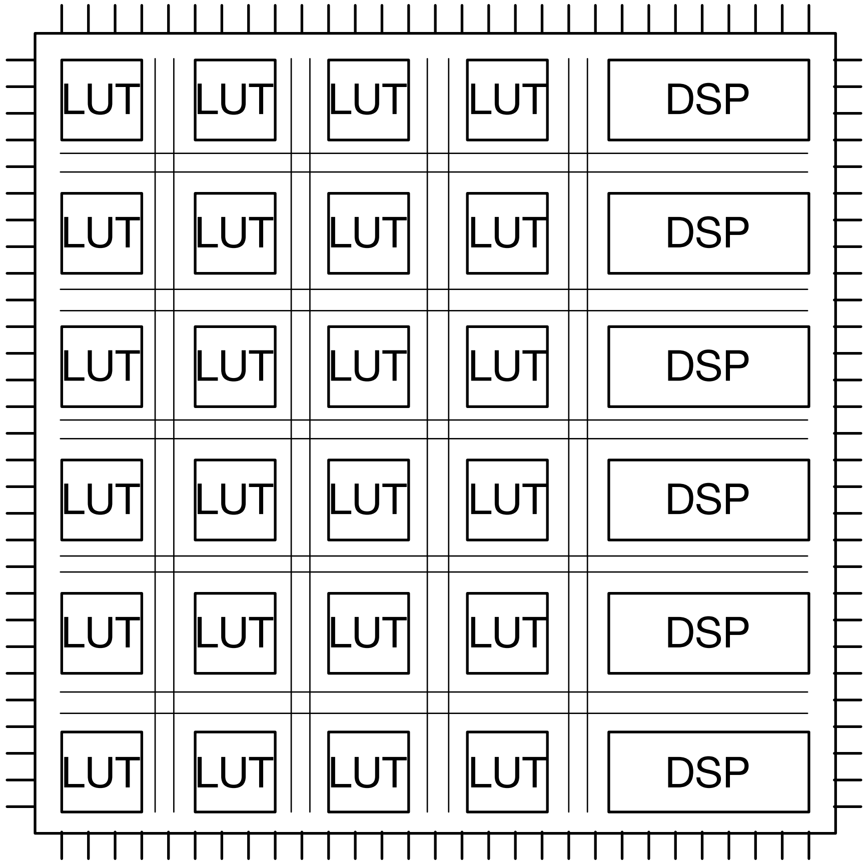

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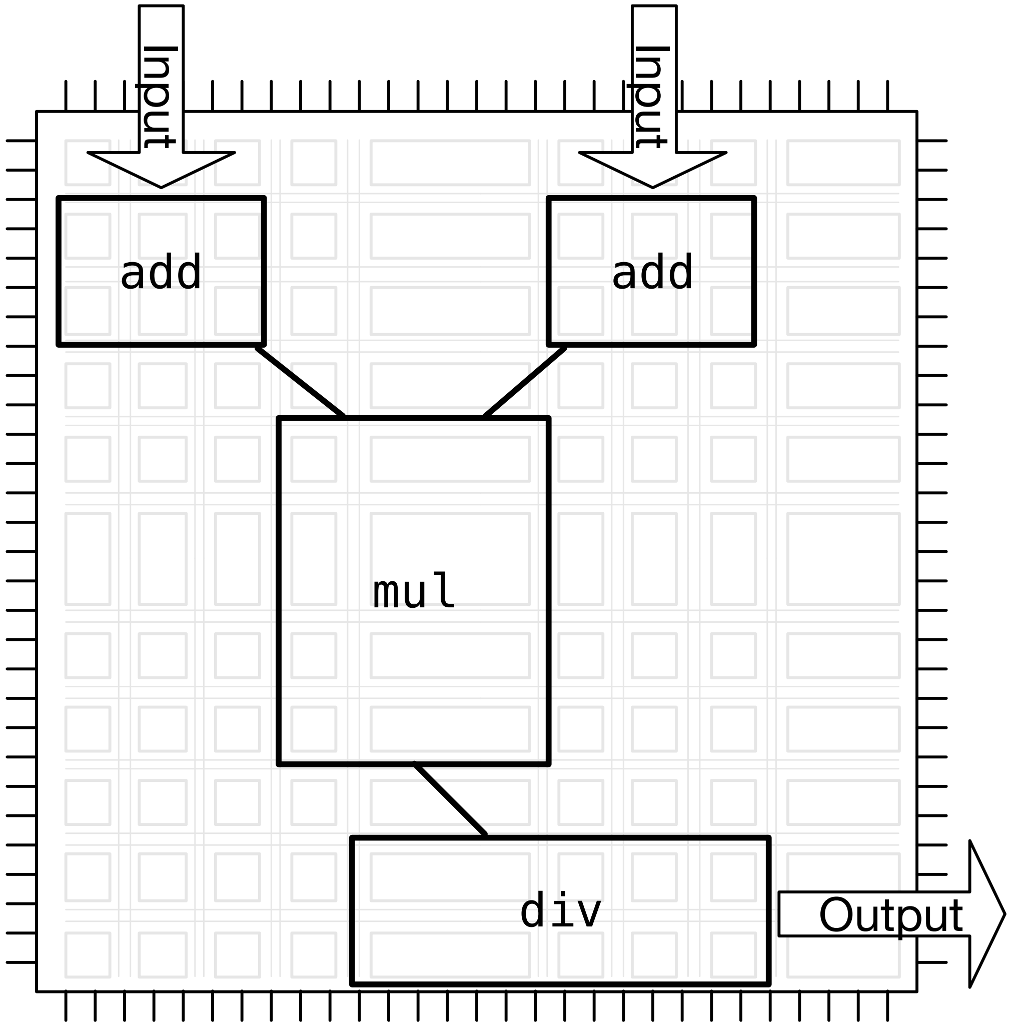

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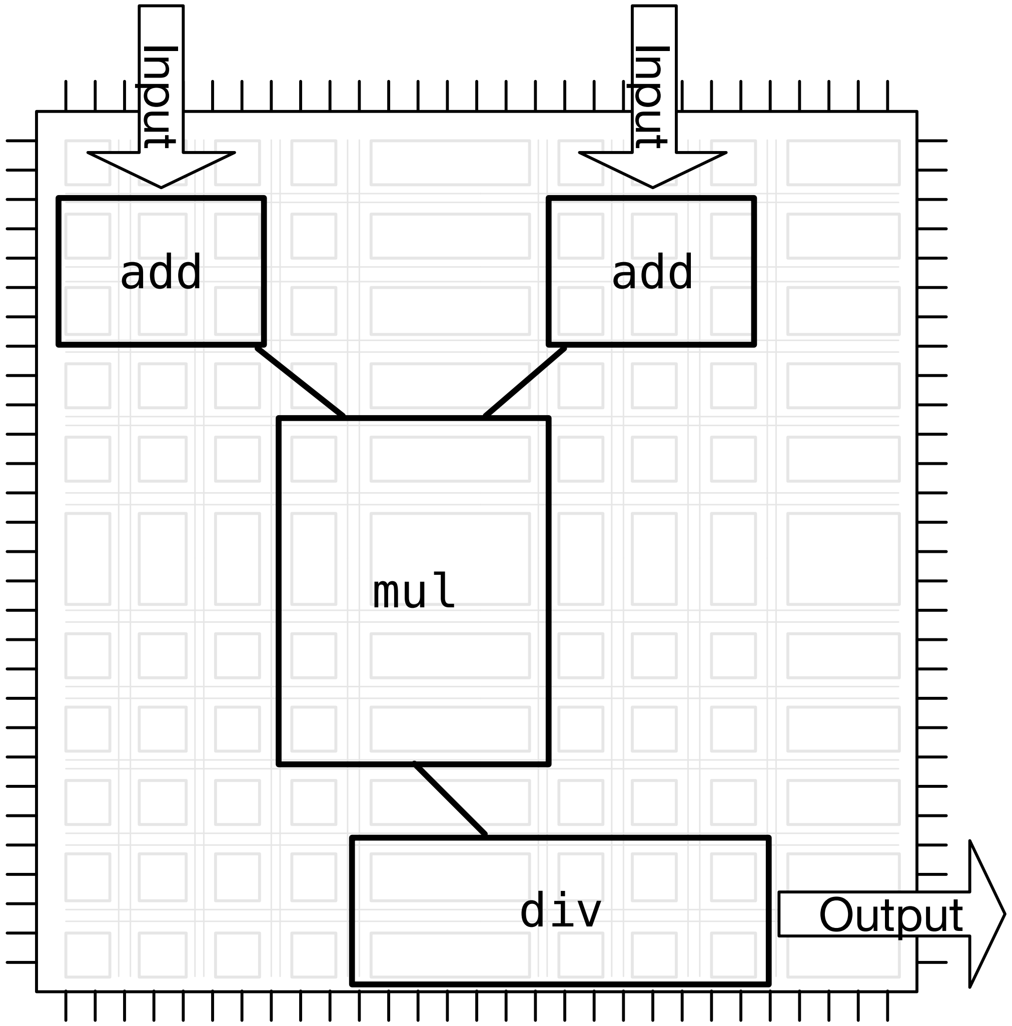
- Connect operators to form a datapath
- Manual design in hardware description language is tedious



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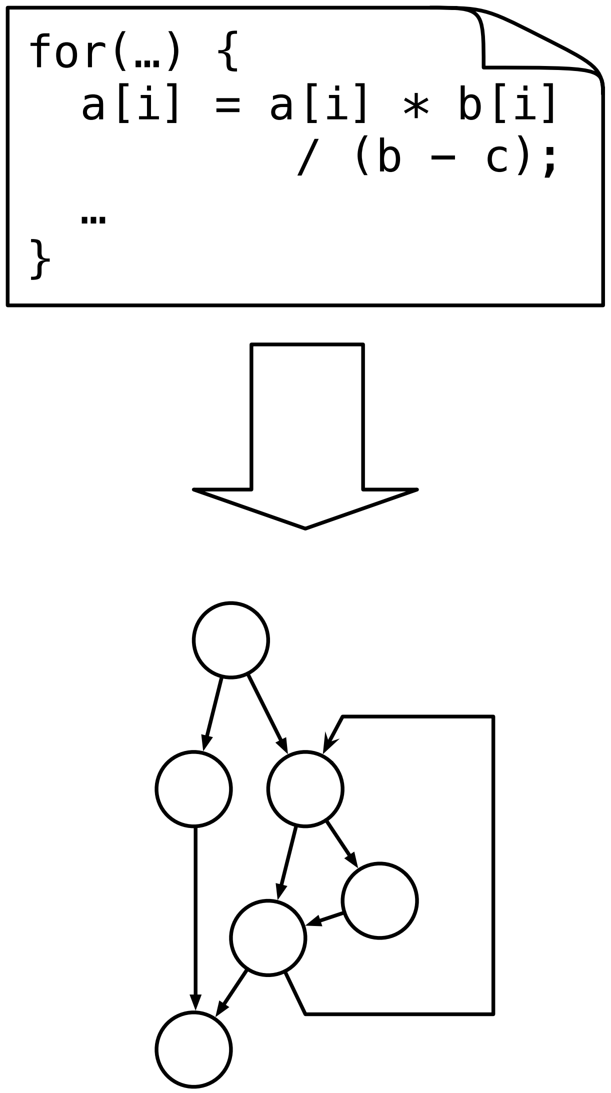

```
for(…) {
  a[i] = a[i] * b[i]
           / (b - c);
  …
}
```

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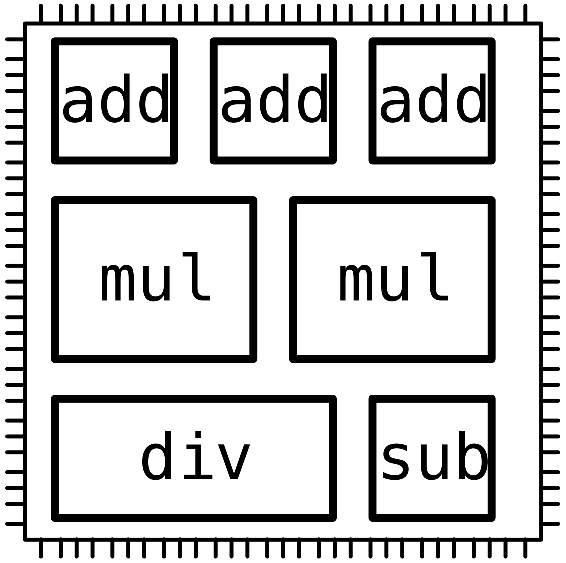

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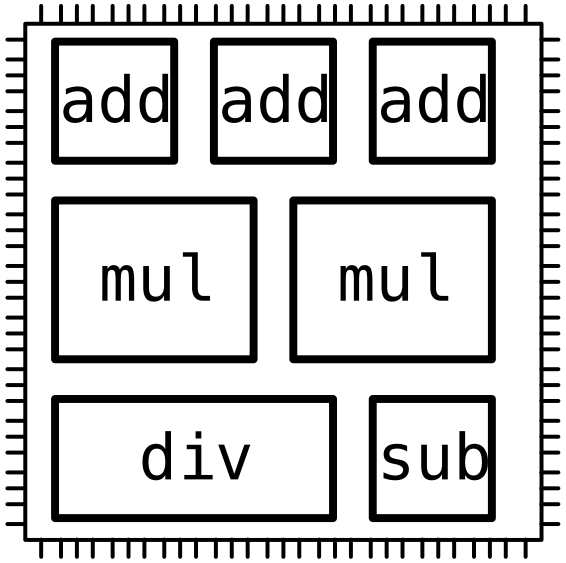

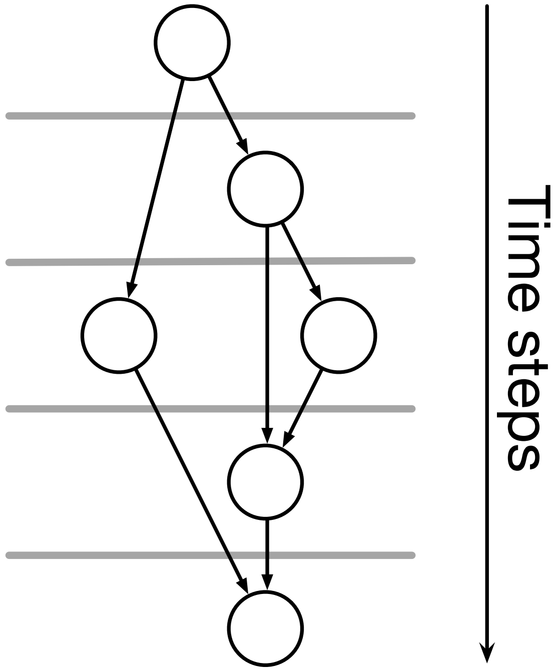

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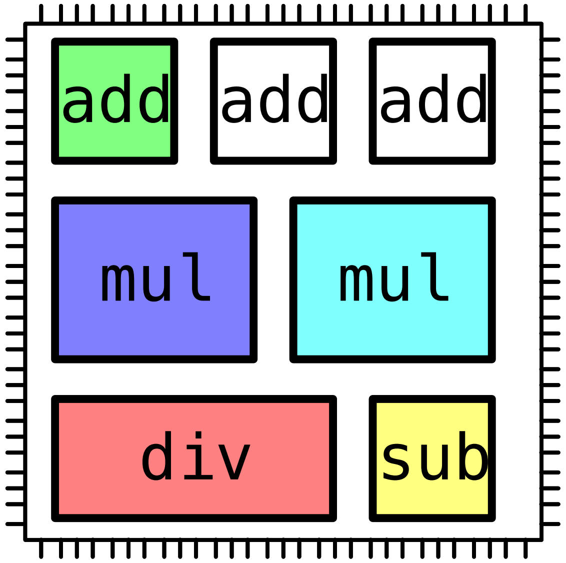
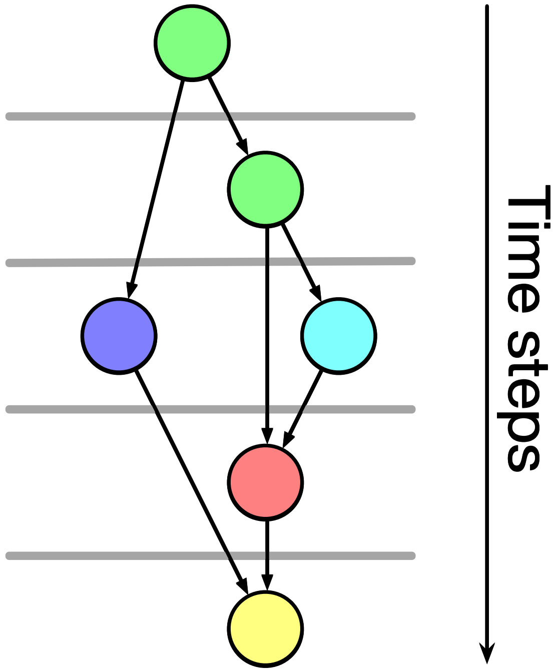
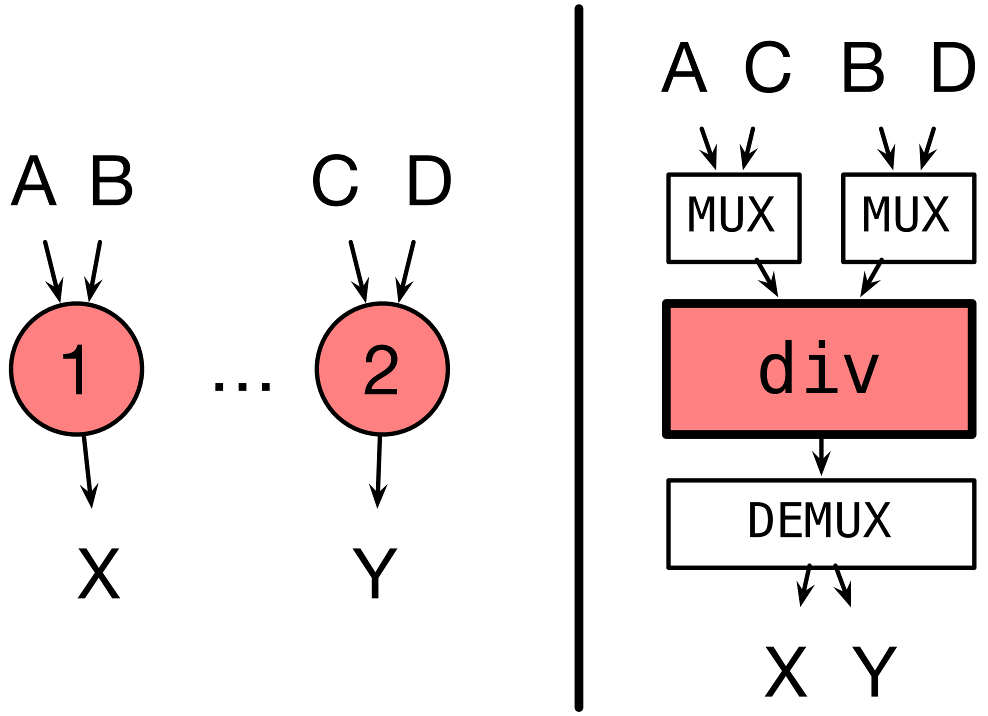
  - Allocation — *how many operators?*
  - Scheduling — *when is an operation executed?*
  - Binding — on which operator?





Key HLS Techniques

- **Operator sharing** = *reduce* resource demand by multiplexing



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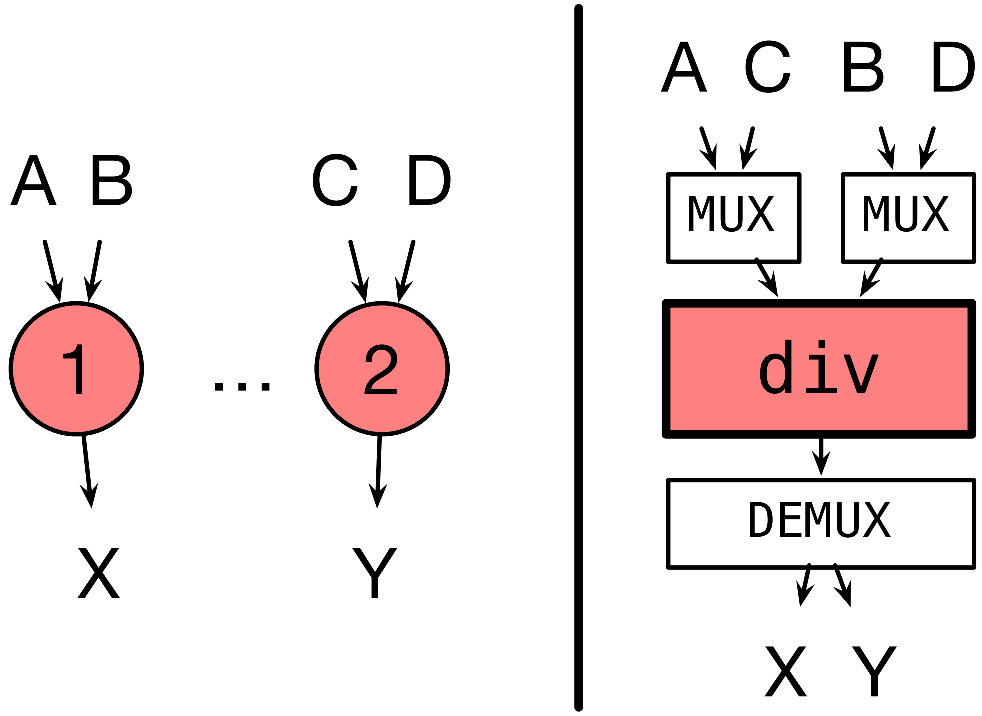

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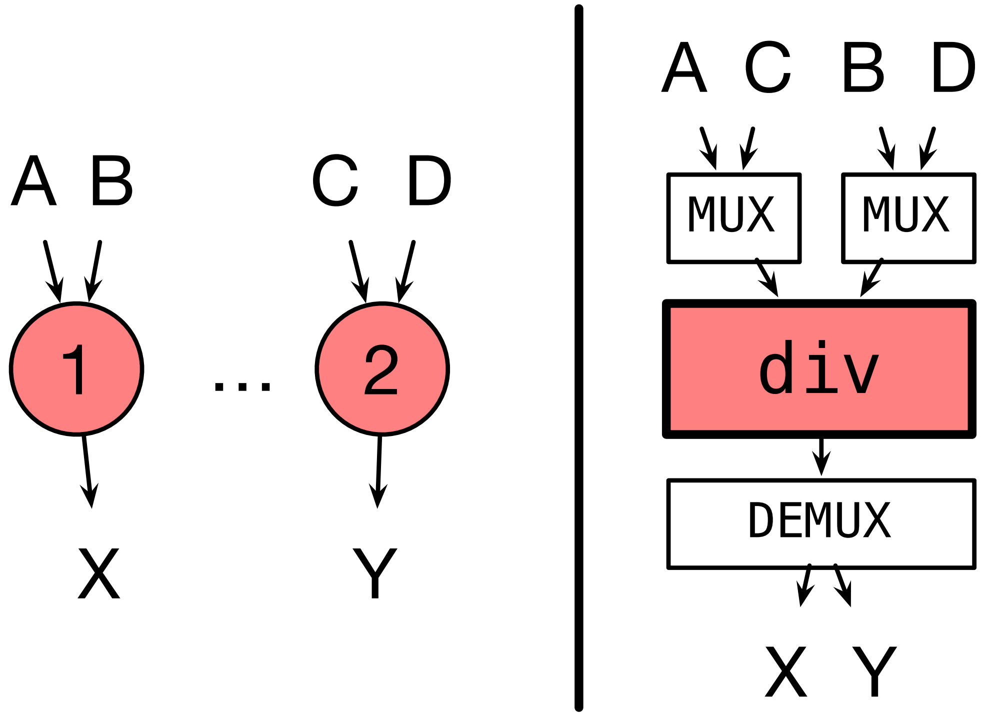
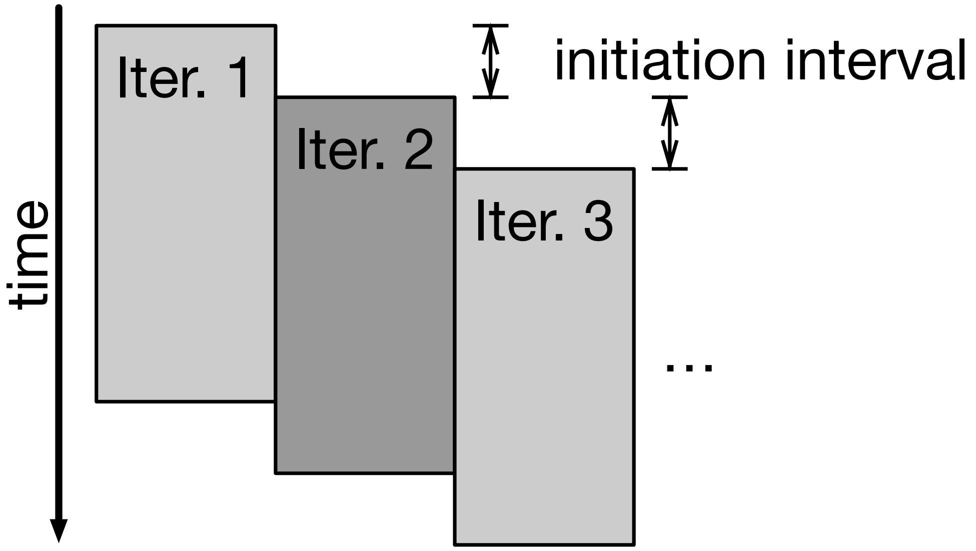


- **Loop pipelining** = *reduce* execution time by overlapping iterations



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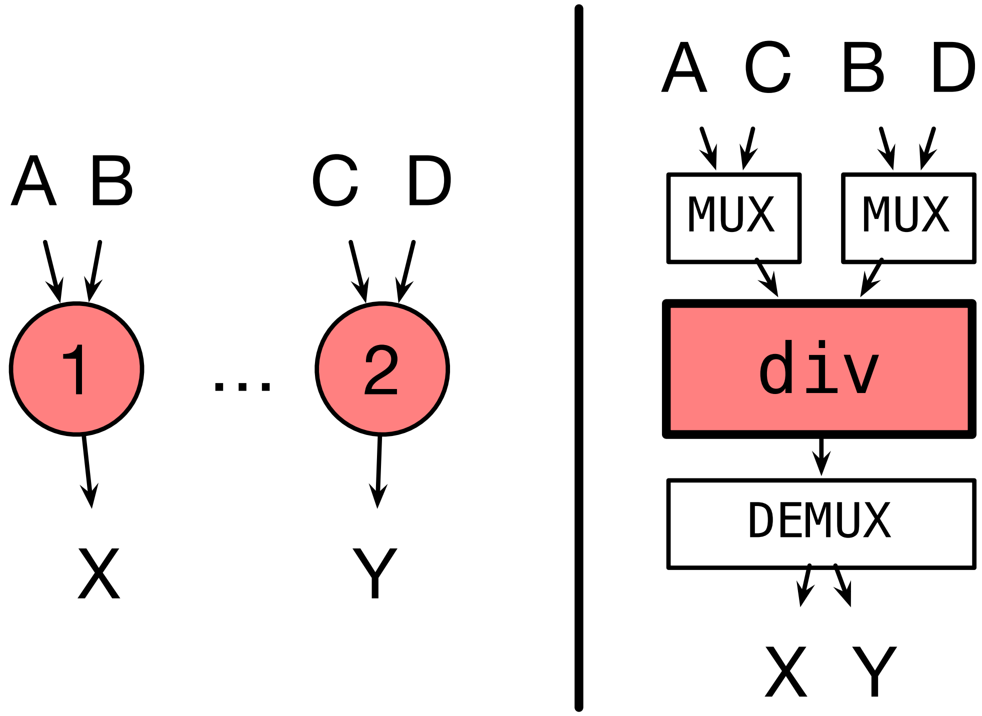

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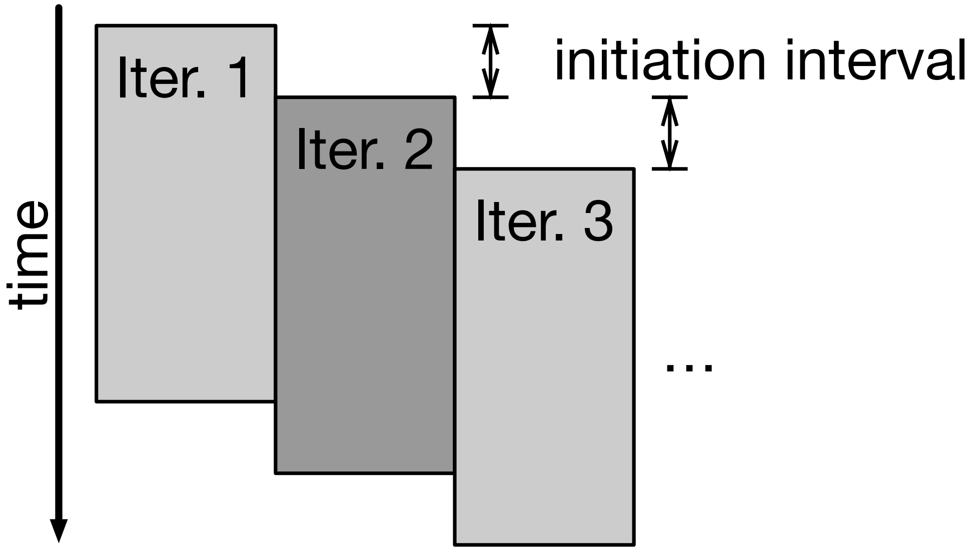
    ⇔

    shorter execution times, more overlap, but less sharing



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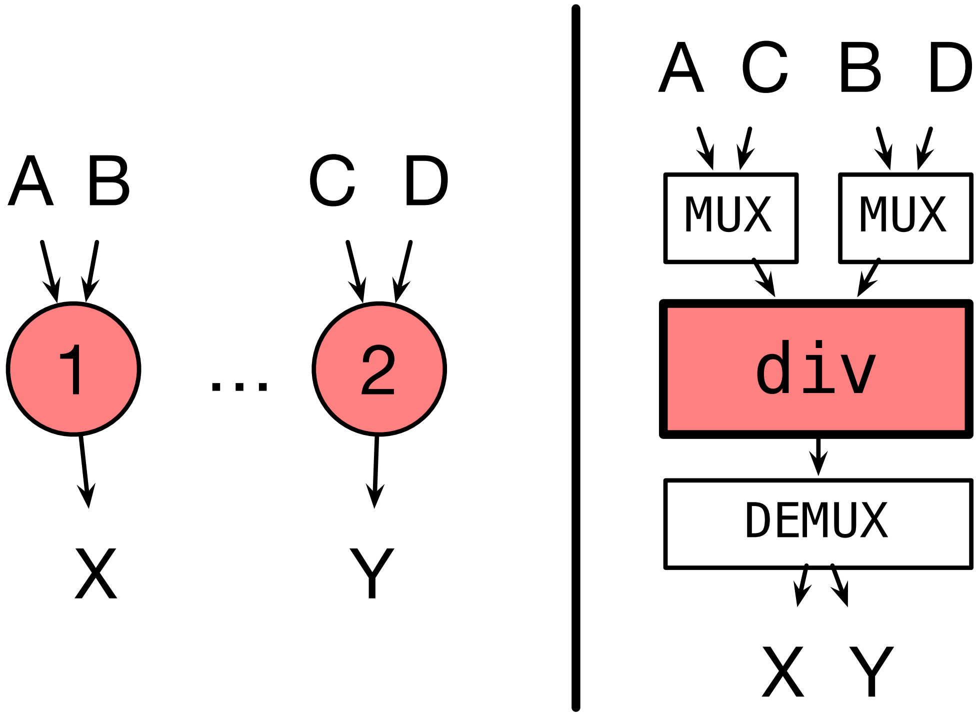
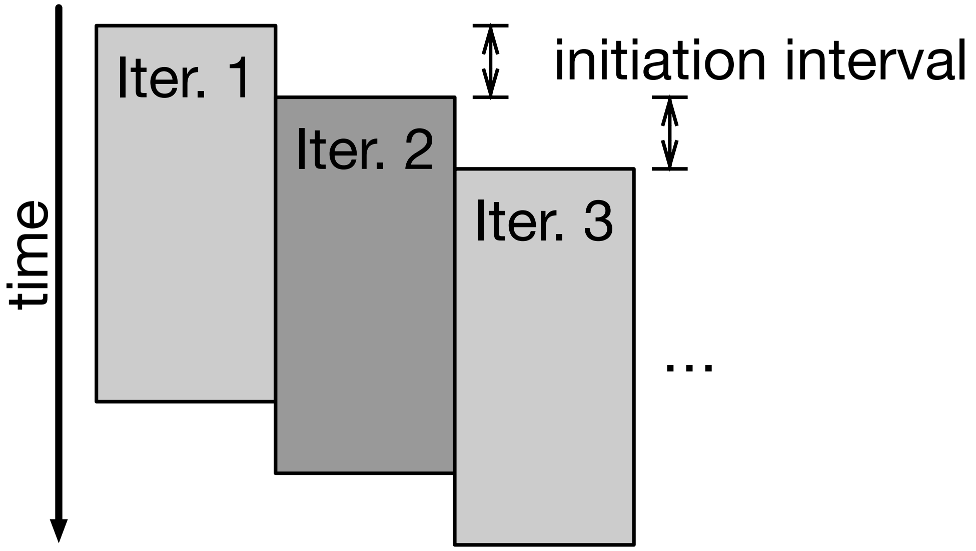


- **Loop pipelining** = *reduce* execution time by overlapping iterations
  - smaller **initiation interval** (II) ⇔ shorter execution times, more overlap, but less sharing
  - enabled by **modulo schedulers**



Motivation

- HLS can construct many different microarchitectures from the same input specification
  - **Conflicting** objectives

$$\begin{array}{ll} \textit{min} & \textit{initiation interval} \\ \textit{min} & \textit{resource utilisation} \end{array}$$

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  - *why not directly as part of the HLS algorithms?*

Contributions

ILP = Integer Linear Program

1. A **framework** for
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   - extends existing ILP-based formulations to **combine** allocation and modulo scheduling

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Binding is guaranteed to exist for typical HLS operators

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1. A **framework** for Resource-Aware Modulo Scheduling (RAMS)
   - extends existing ILP-based formulations to **combine** allocation and modulo scheduling

Binding is guaranteed to exist for typical HLS operators

2. We investigate ways to efficiently compute different trade-off solutions

Agenda

□ Introduction to high-level synthesis

▶ **Resource-aware modulo scheduling**

□ Exploration of trade-off solutions

□ Experimental evaluation

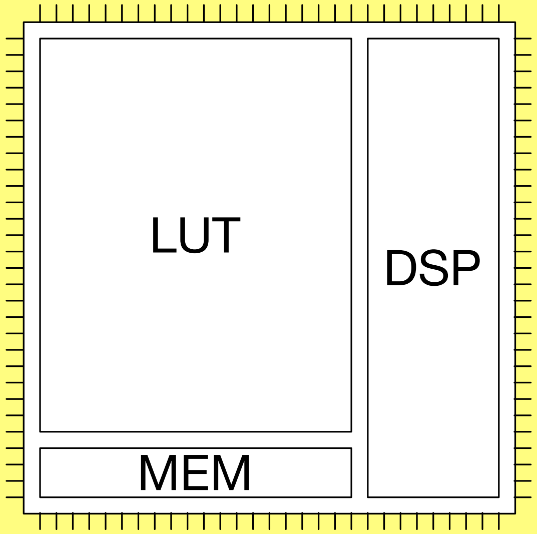
Problem Signature

🟨 = resource-aware extension

Input:

Resource types

R



each $r \in R$ provides N_r elements

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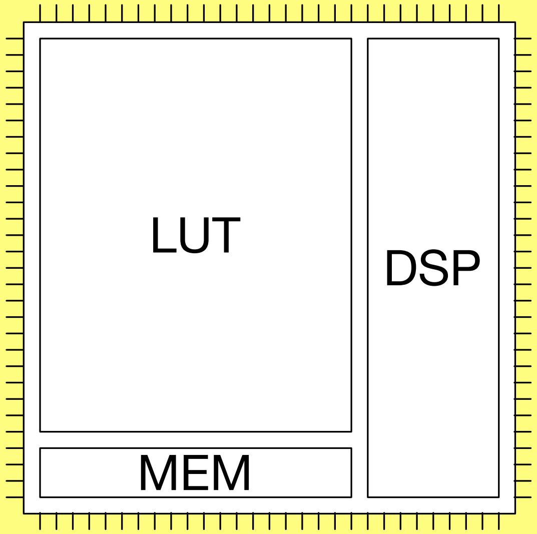

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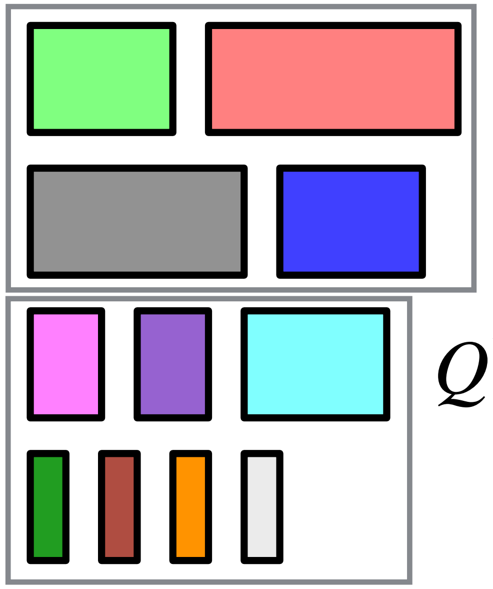

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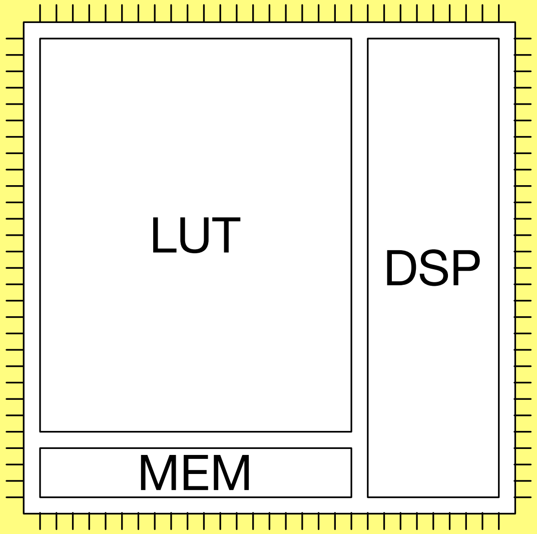

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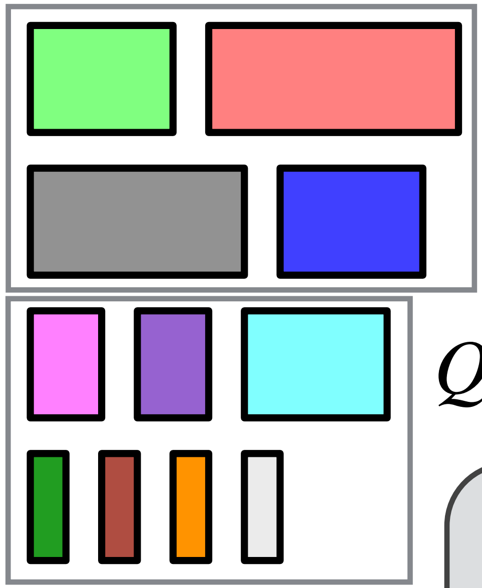

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…too „cheap“
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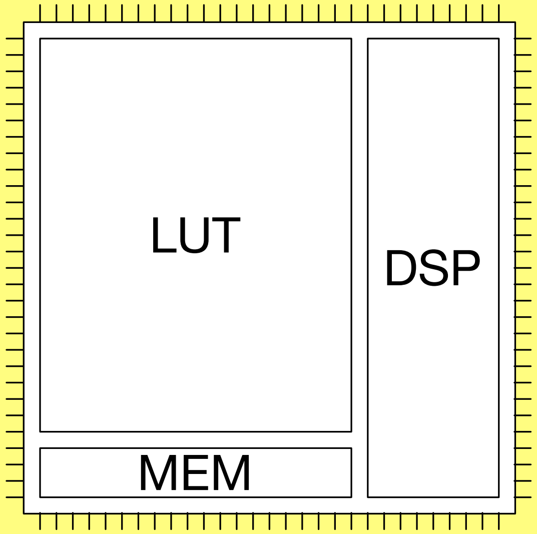

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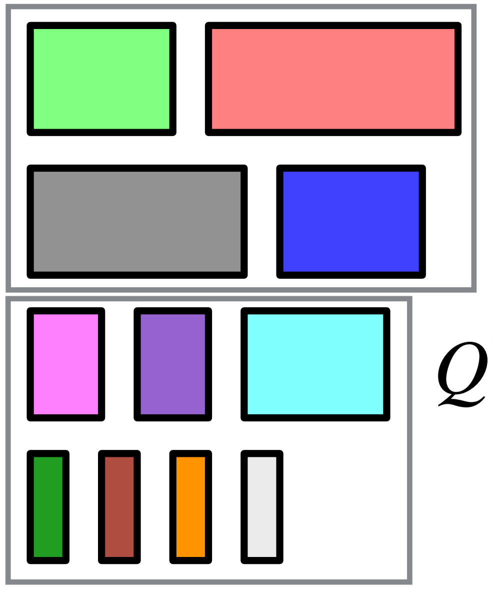

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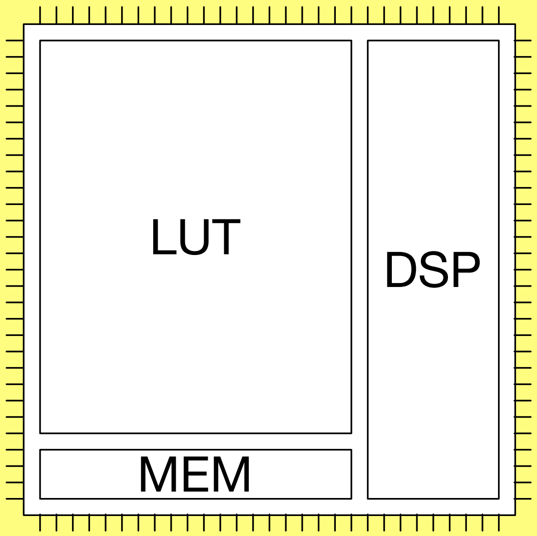

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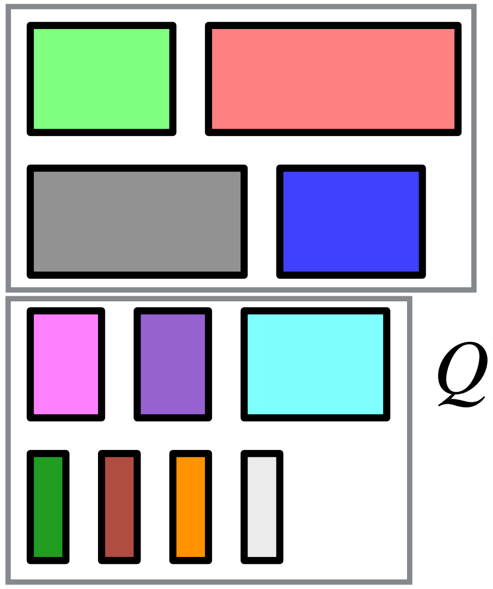

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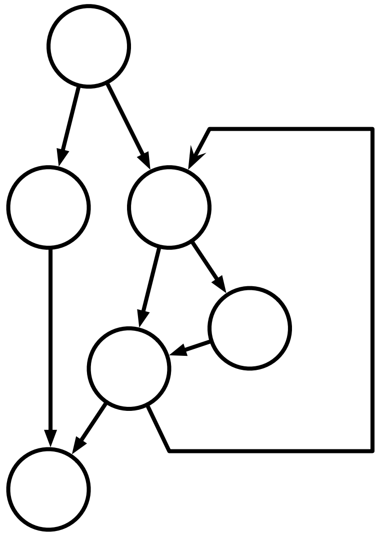
Dependence graph

$G = (O, E)$



subsets O_q group operations using operator type q

each $i \rightarrow j \in E$ has a distance β_{ij}

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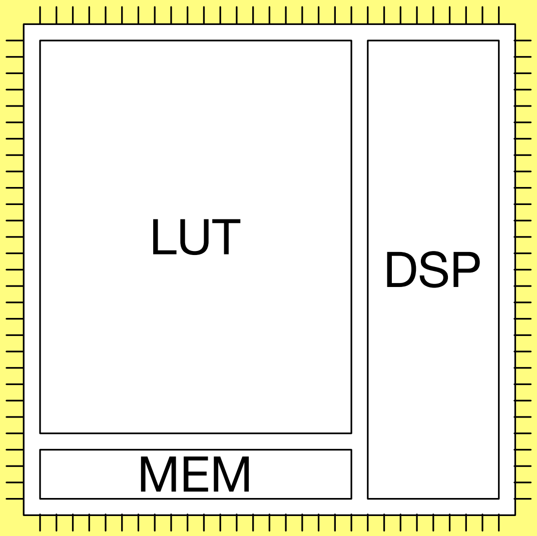

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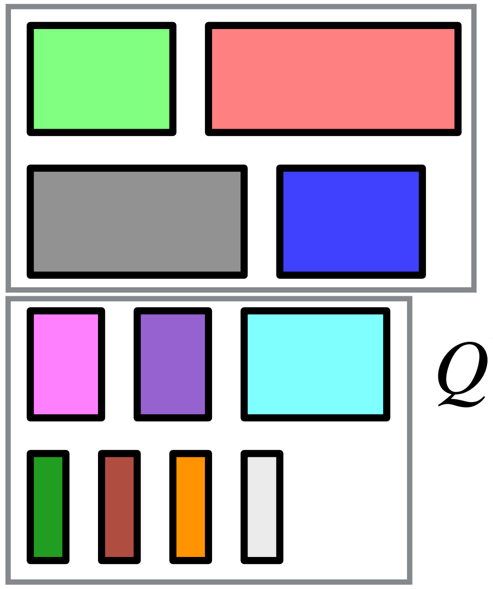

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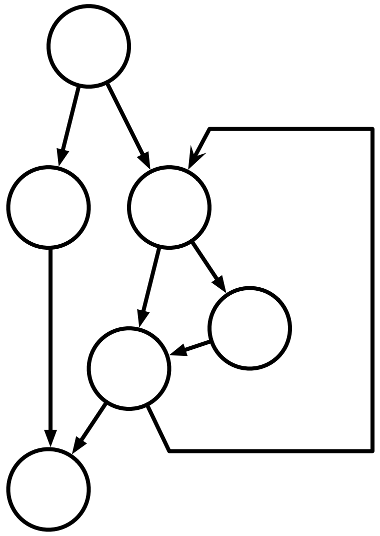

subsets O_q group operations using operator type q

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Output: A solution S, comprised of:

II^S initiation interval

t_i^S start times for each operation („schedule“)

a_q^S number of instances for each operator type („allocation“, A^S)

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🟨 = resource-aware extension

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3. *„the resource demand is within the device capacity“*

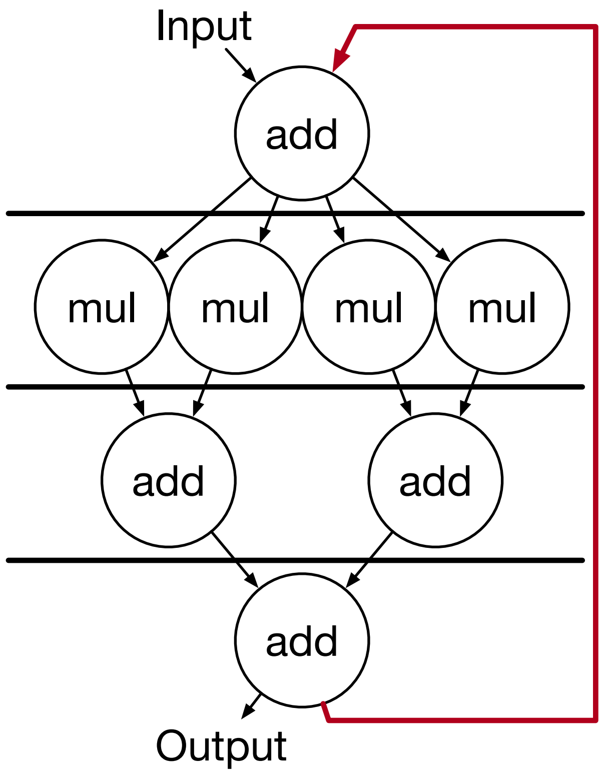
$$\sum_{q \in Q} a_q^S \cdot n_{q,r} \;\leq\; N_r \quad \forall r \in R$$

Trade-offs & (In-)Feasibility

- Example: Different trade-offs

Trade-offs & (In-)Feasibility

II=1 latency=4
4 mul 3 add



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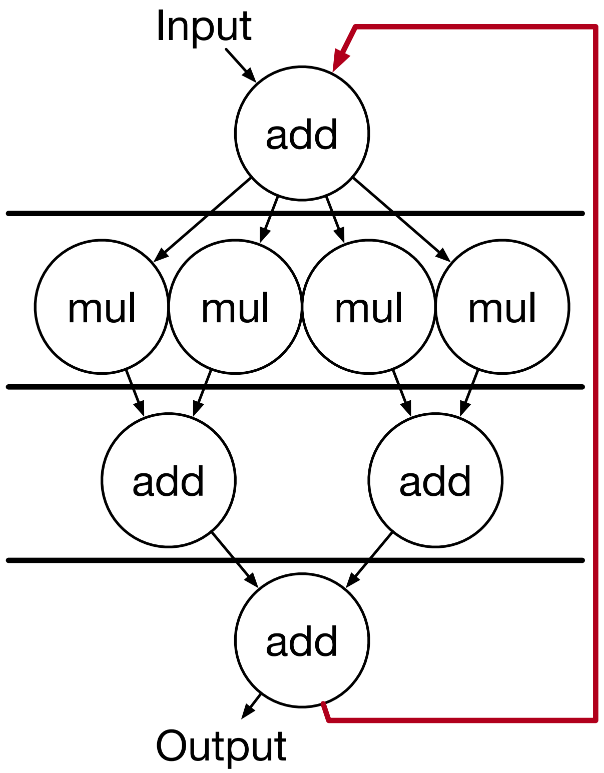

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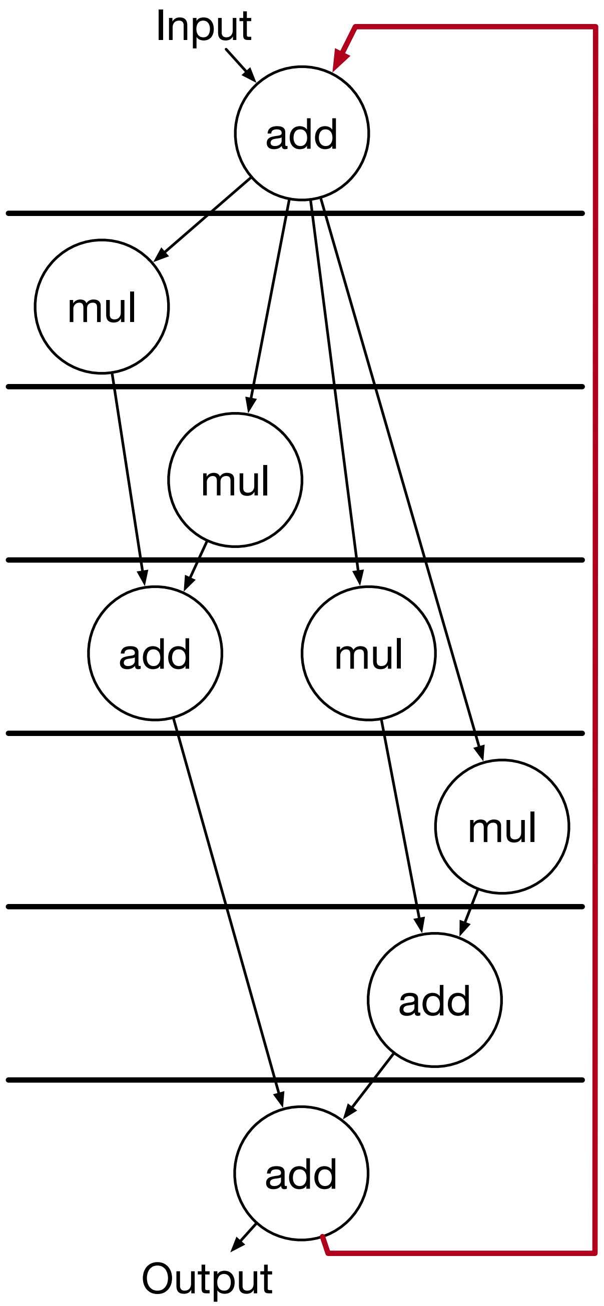

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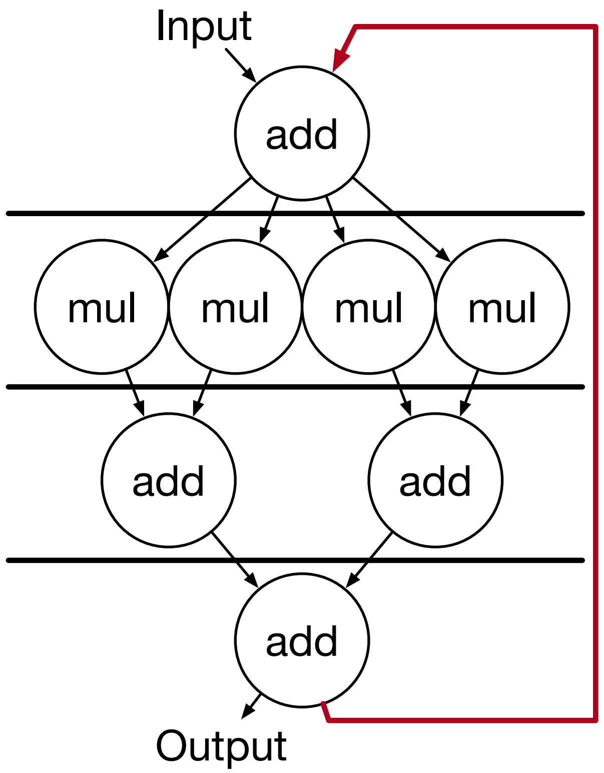

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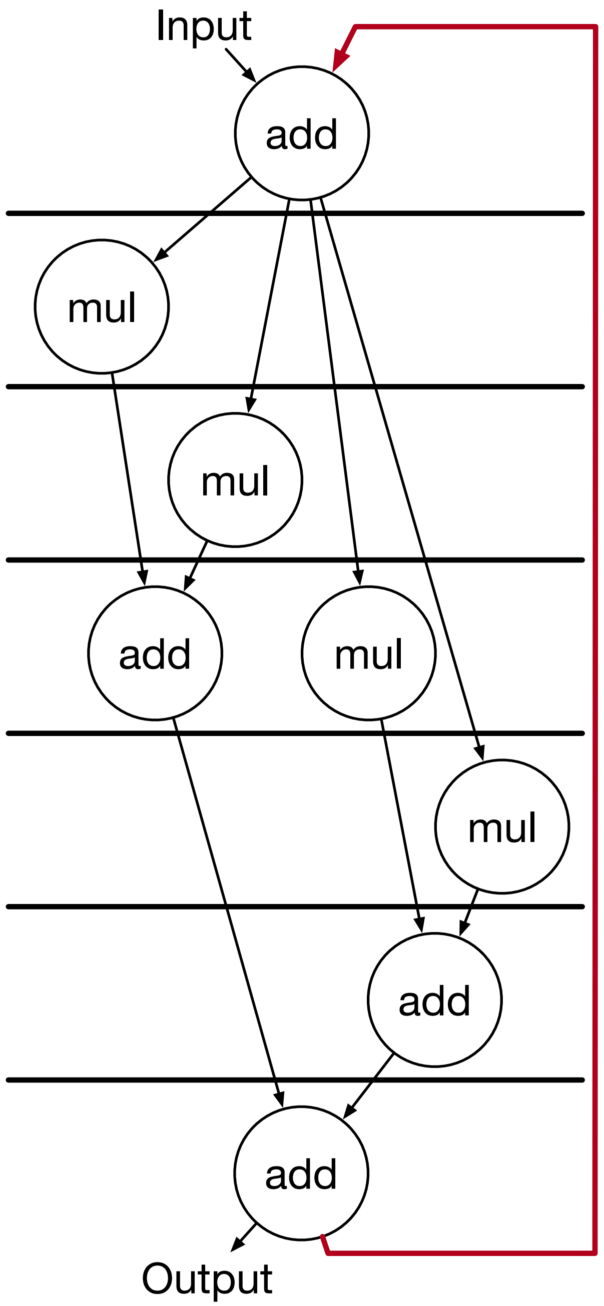

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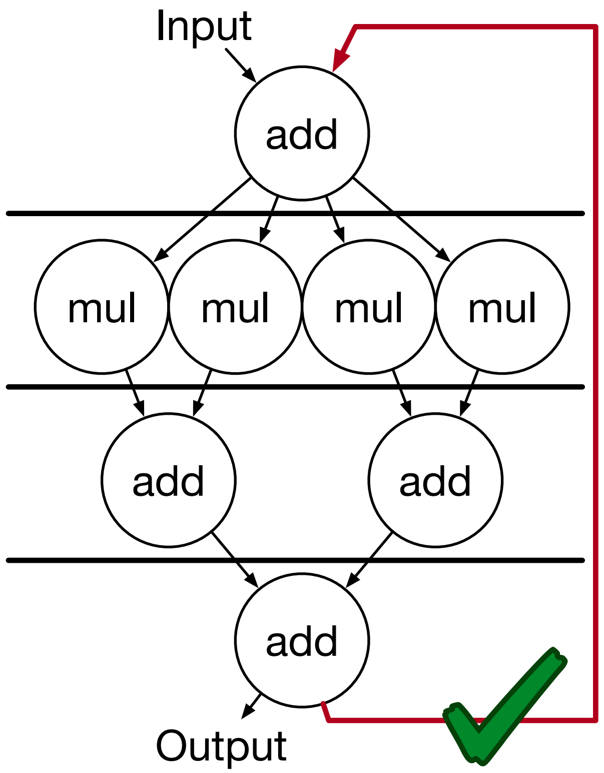

Inter-iteration dependence

- Example: Different trade-offs
- *Isn’t there an II to makes any allocation feasible (& vice versa)?*
- Not if an operation is subject to a **deadline**
  - Inter-iteration dependences „`a[i] = f(a[i-4])`“

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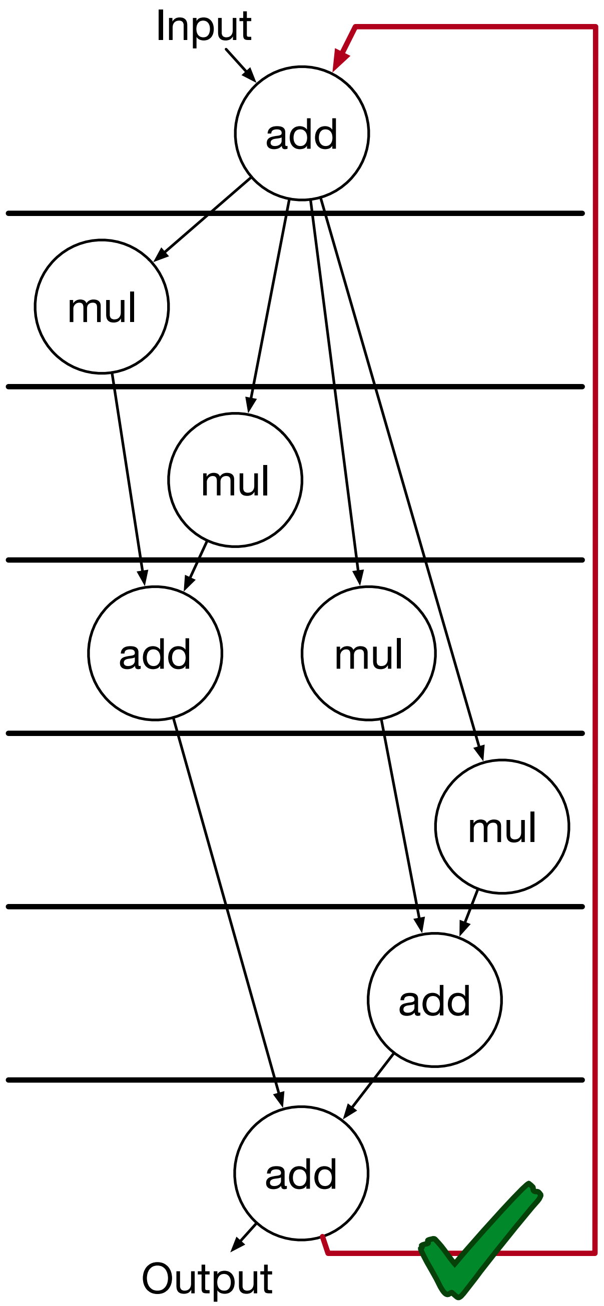

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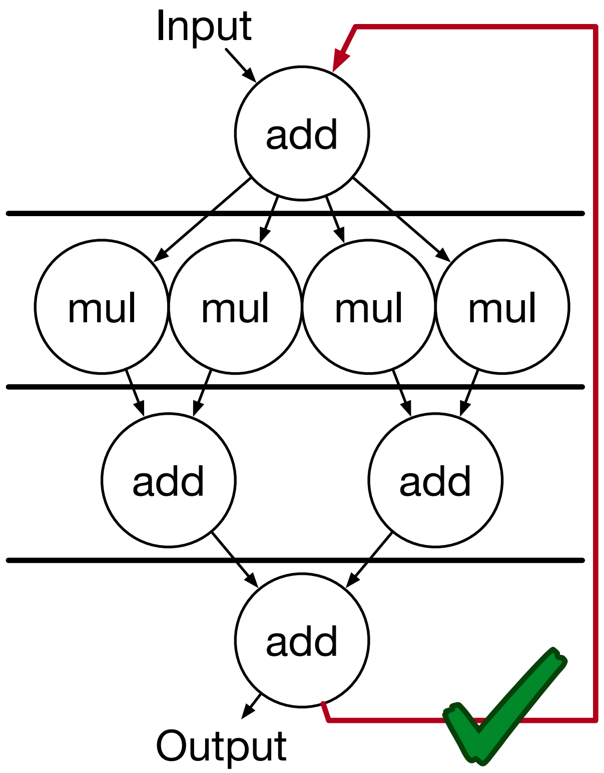
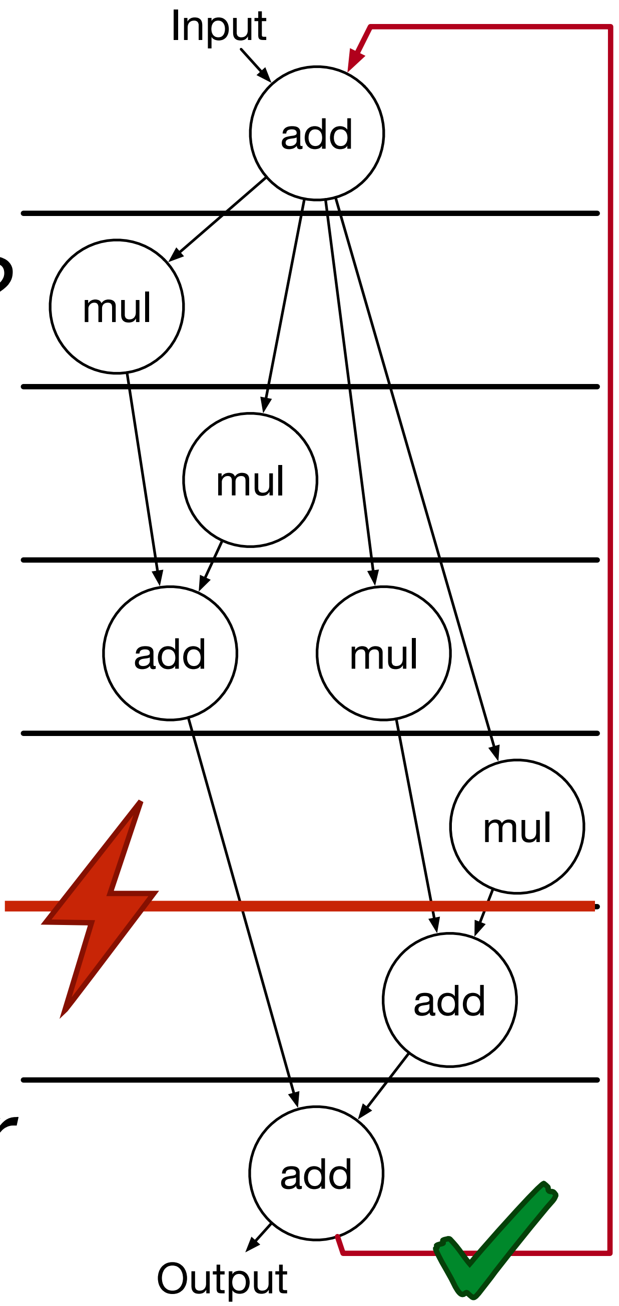


Inter-iteration dependence

External latency constraint

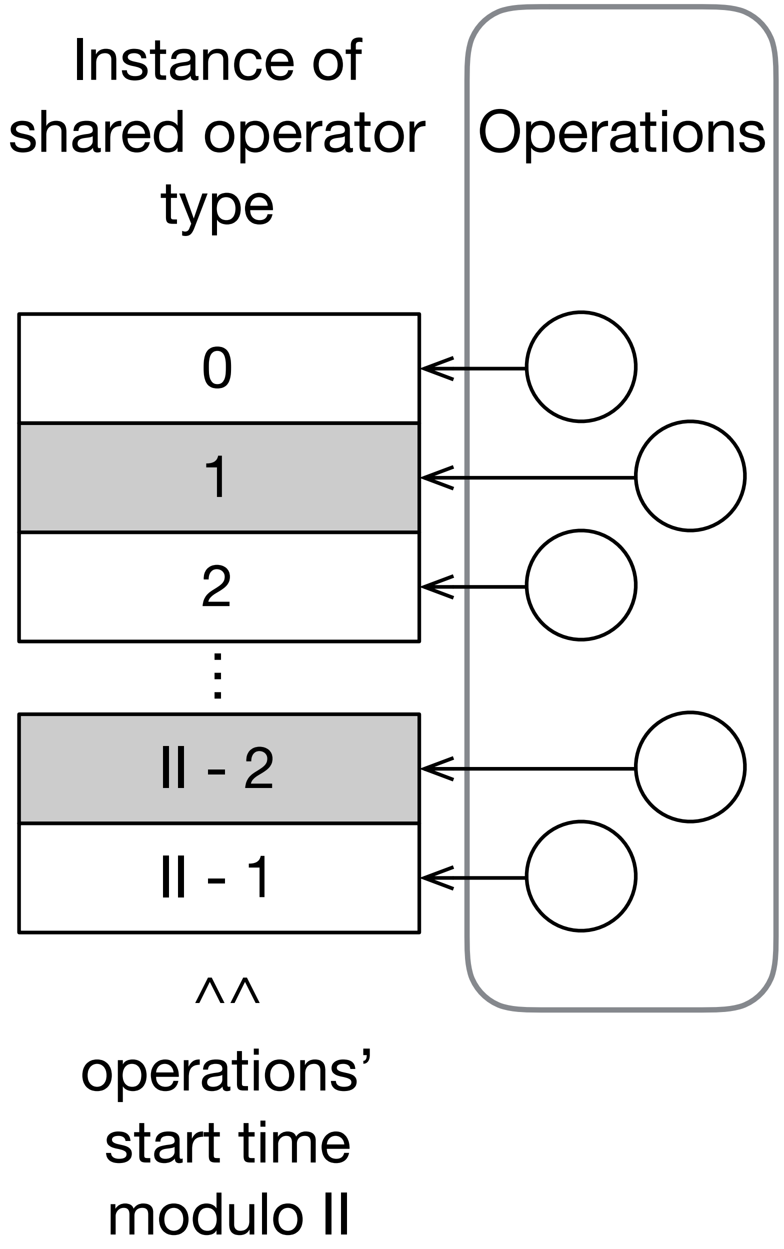
- Example: Different trade-offs
- *Isn’t there an II to makes any allocation feasible (& vice versa)?*
- Not if an operation is subject to a **deadline**
  - Inter-iteration dependences „`a[i] = f(a[i-4])`“
  - External latency constraints *„output must be available after 5 cycles“*

II=4 latency=7
1 mul 1 add



Trivial Allocation

- One operator provides II-many slots


Instance of shared operator type
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⋮
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operations' start time modulo II

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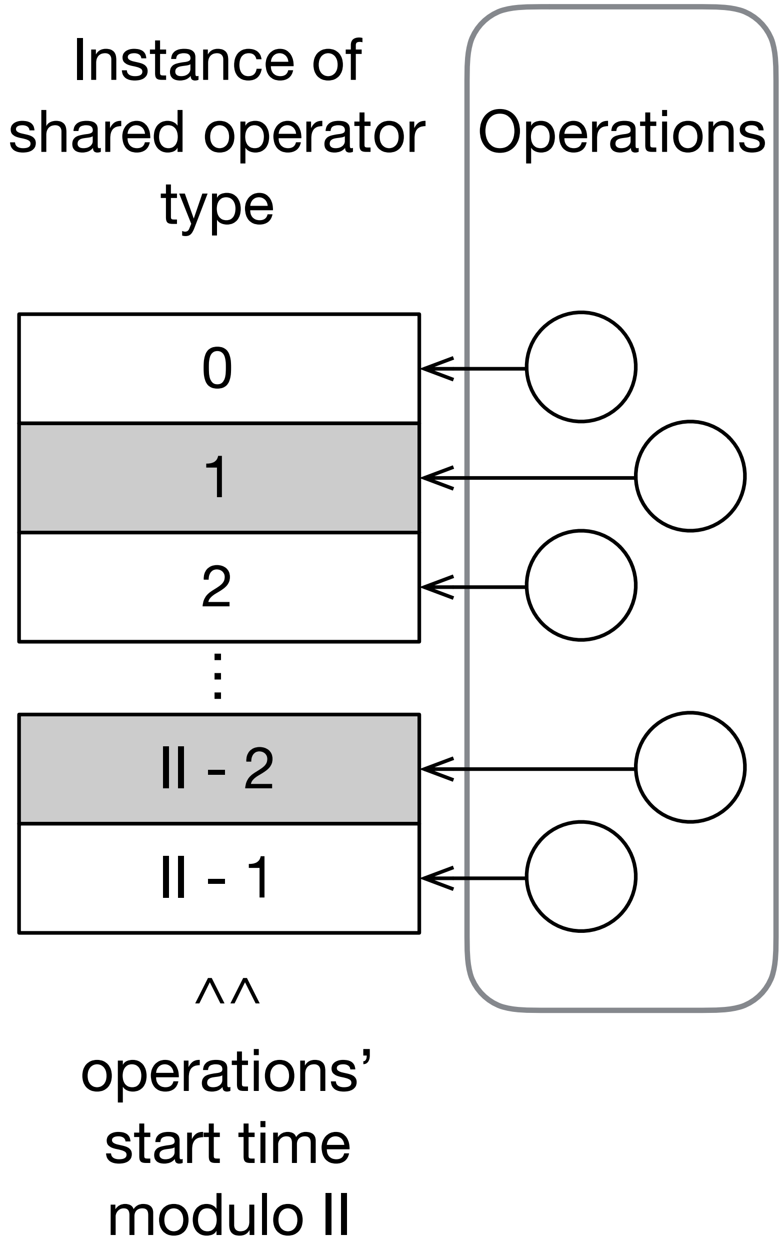

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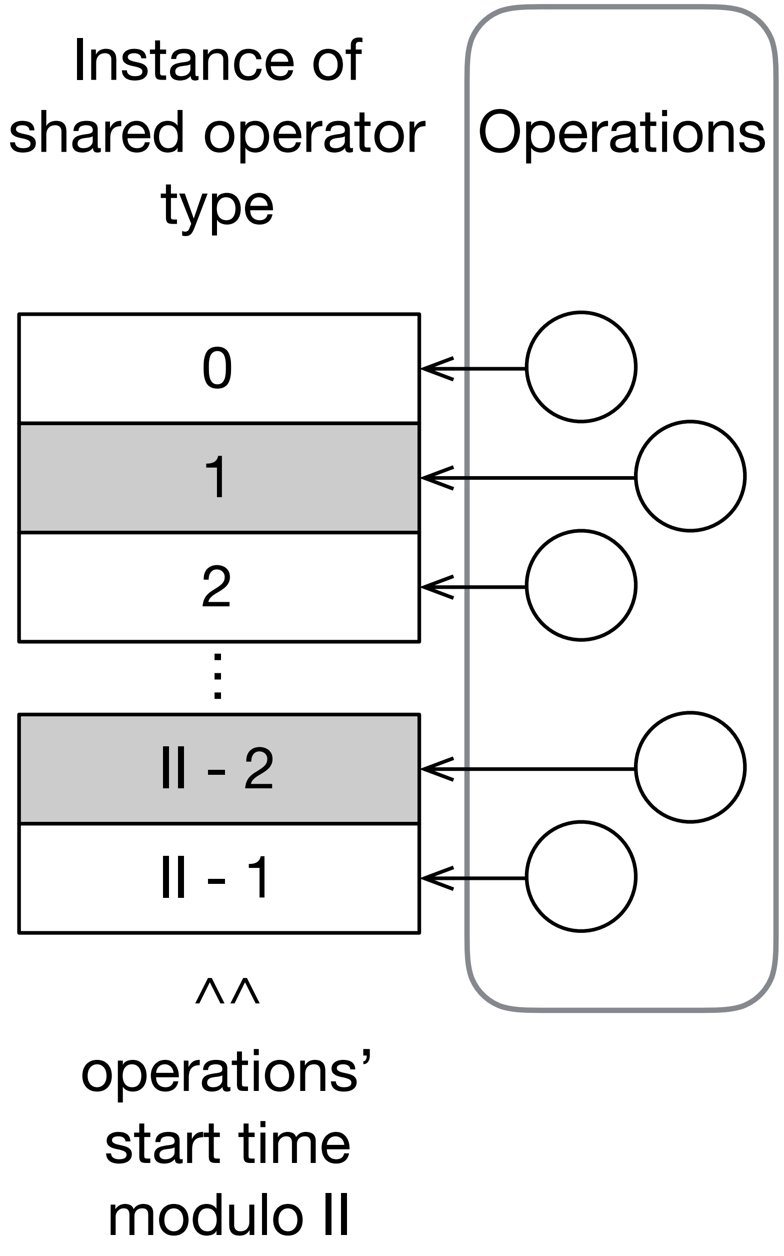
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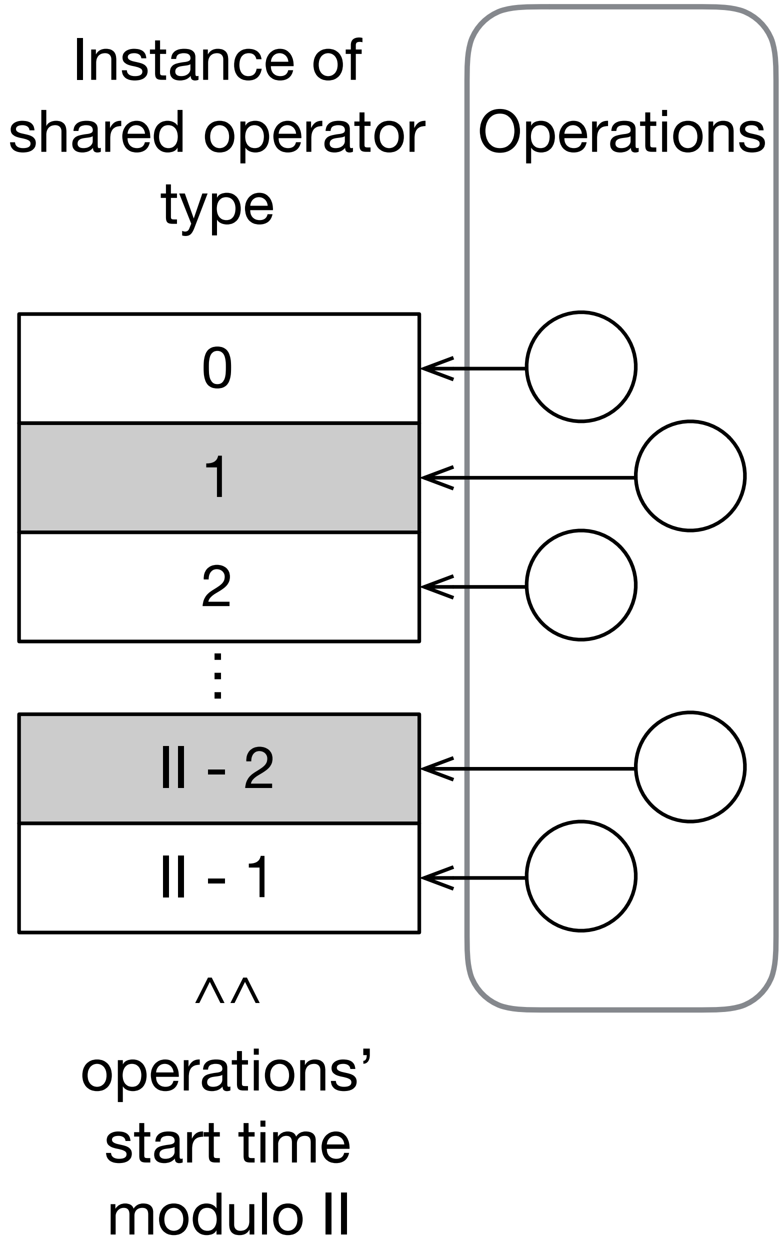
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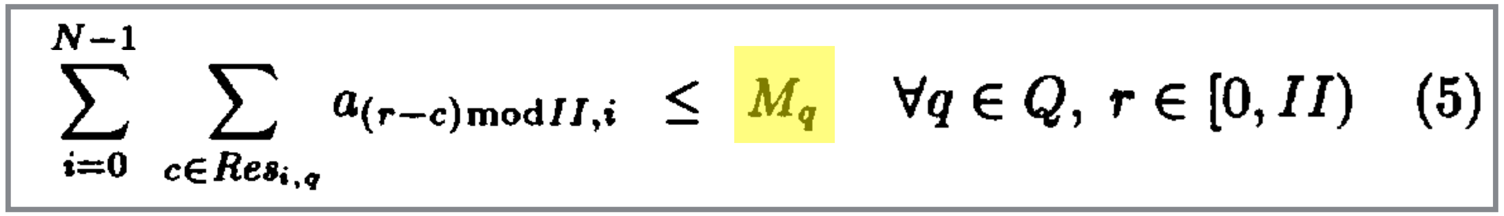

$$\sum_{i=0}^{N-1} \sum_{c \in Res_{i,q}} a_{(r-c)\mathrm{mod}\,II,i} \leq M_q \quad \forall q \in Q,\ r \in [0, II) \quad (5)$$

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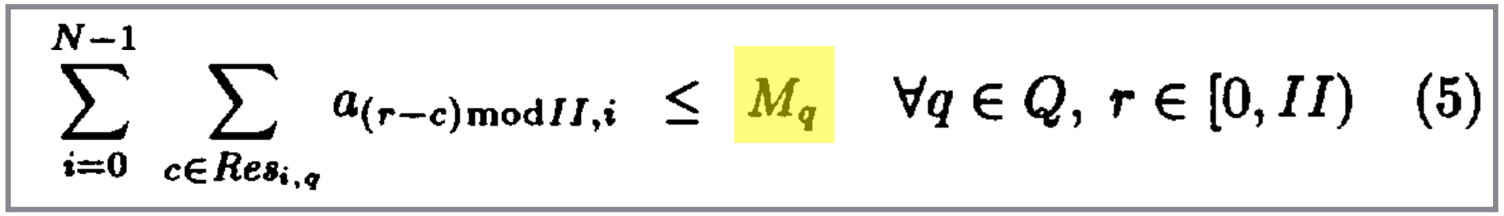

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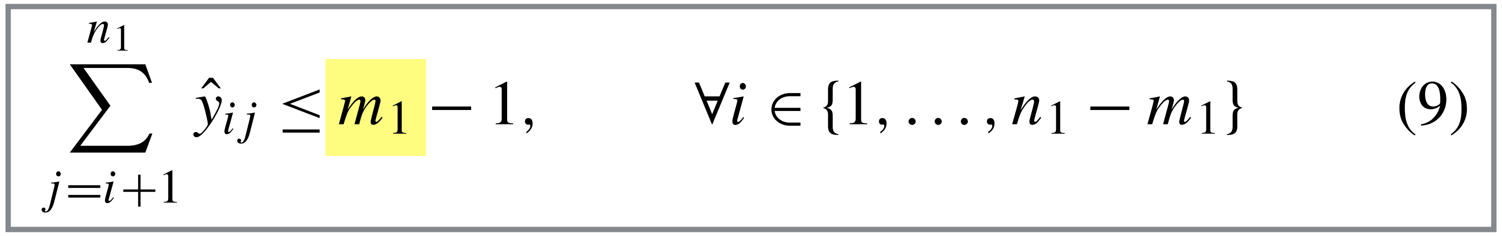

$$\sum_{j=i+1}^{n_1} \hat{y}_{ij} \le m_1 - 1, \qquad \forall i \in \{1, \ldots, n_1 - m_1\} \tag{9}$$

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  - **MV**: „Moovac“ formulation by Oppermann et al. (2019)

$$r_i \leq a_k - 1 \qquad \forall k \in R : \forall i \in L_k \qquad (\mathrm{M11})$$

Agenda

- □ Introduction to high-level synthesis
- □ Resource-aware modulo scheduling
- ▷ **Exploration of trade-off solutions**
- □ Experimental evaluation

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- Given a RAMS problem, the goal is to compute all **Pareto-optimal** solutions
  - i.e. a solution that is **not dominated** by any other solution
  - Example:
    II=3, RU=30% …
    … dominates II=4, RU=40%
    … does not dominate II=2, RU=40%

ε-Approach

- standard method from multi-criteria optimisation

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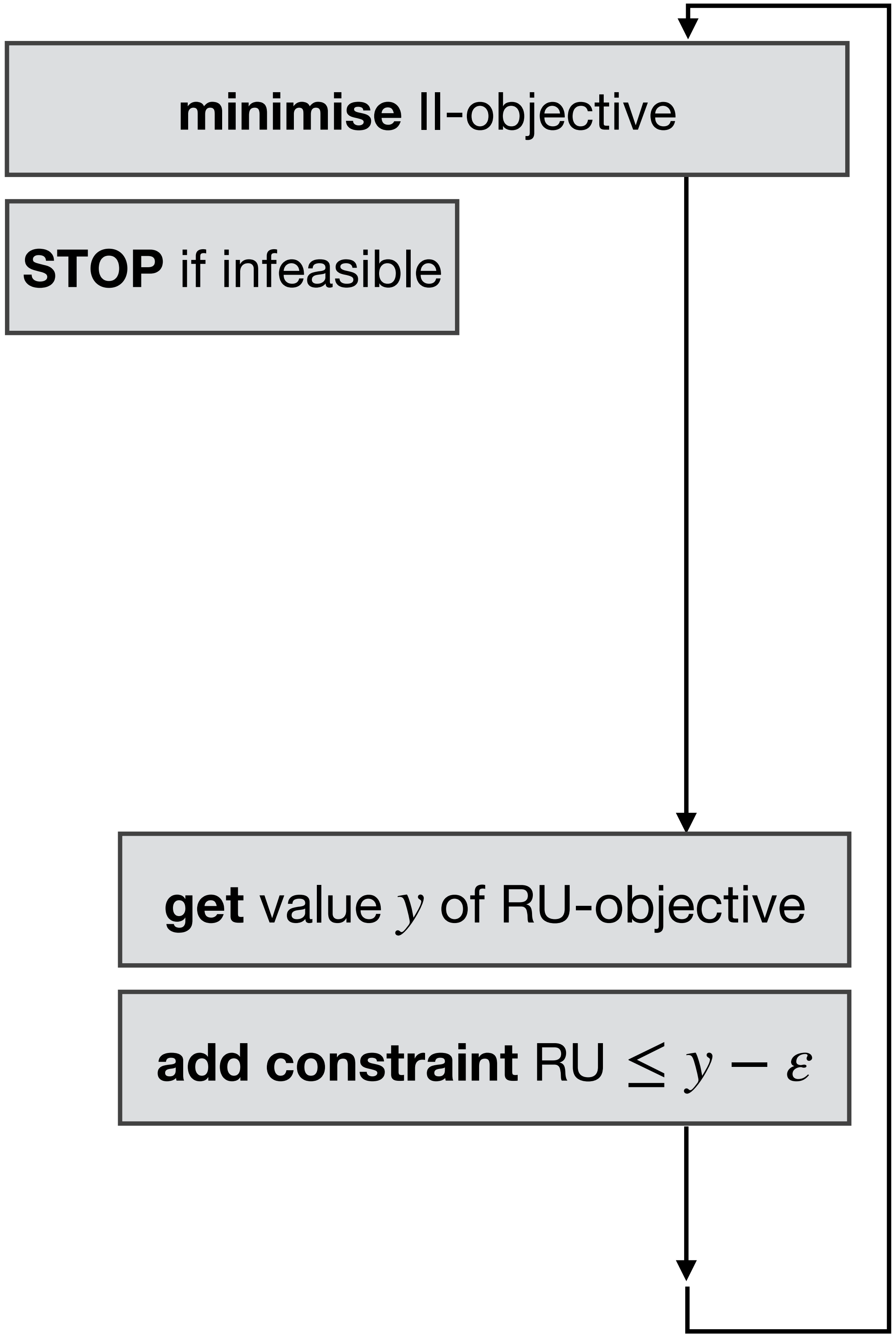
  - basically: optimise one objective, and successively add constraints for the other



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STOP if infeasible

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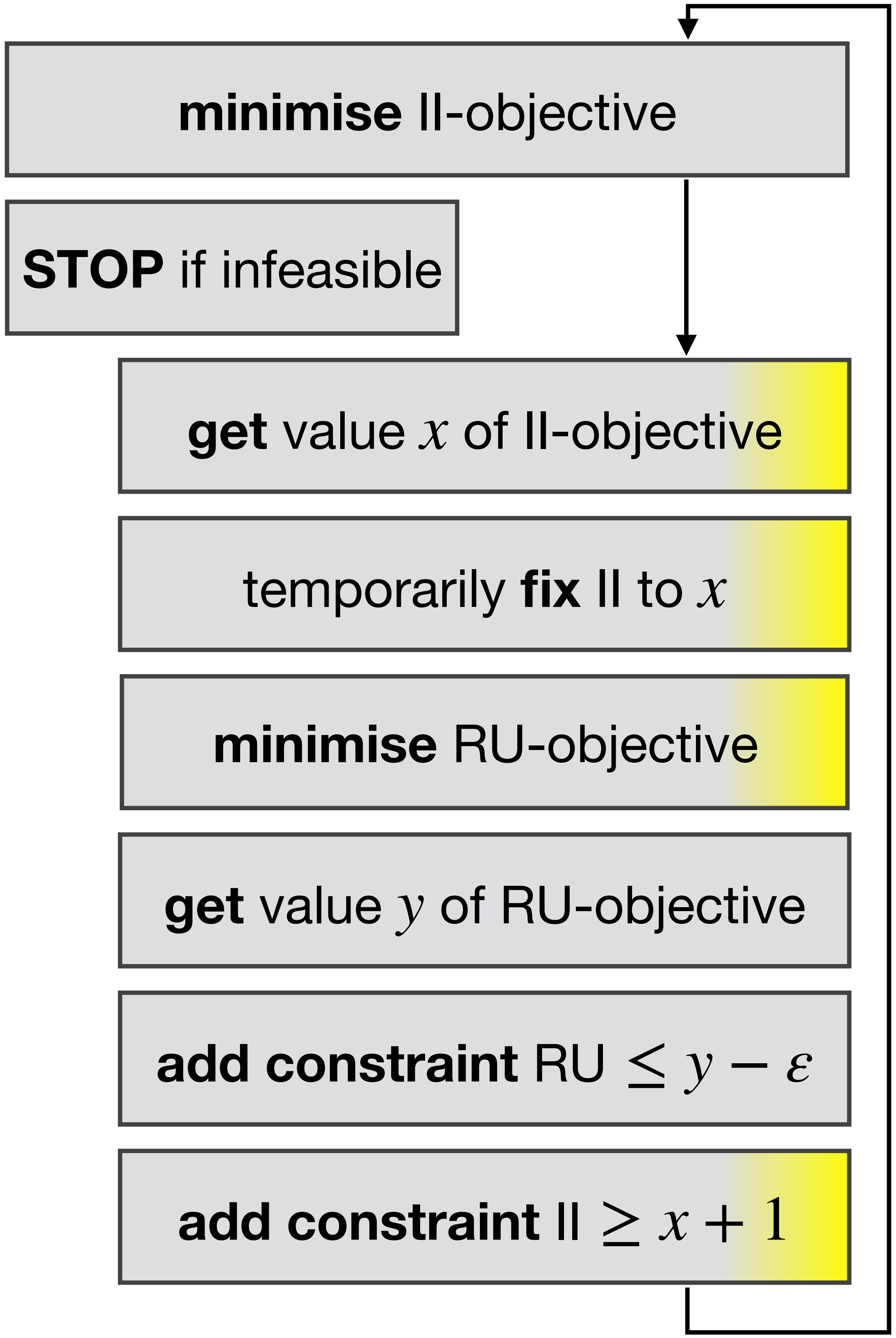

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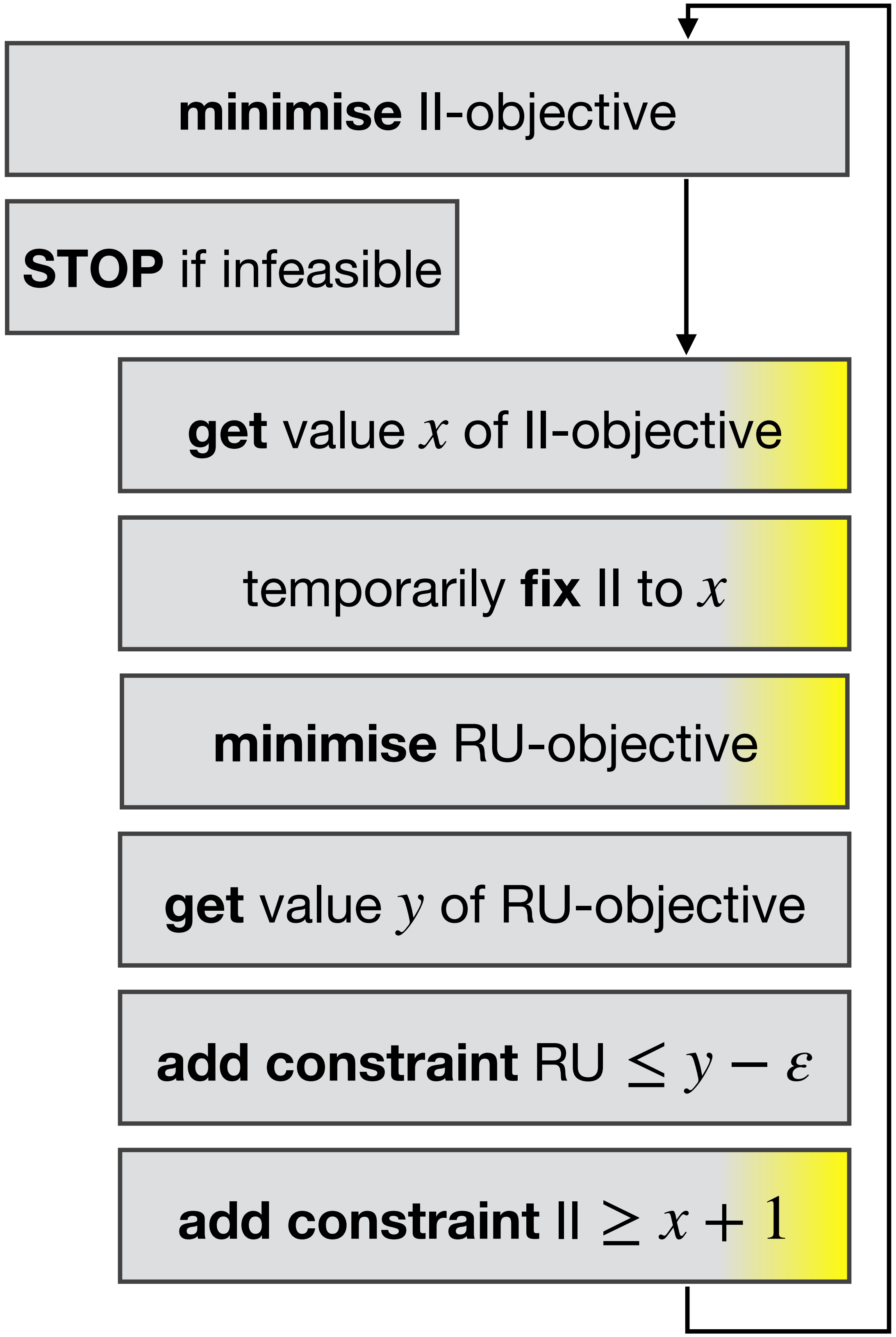
  - basically: optimise one objective, and successively add constraints for the other
  - we minimise both objectives to speed up convergence
  - requires RAMS formulation with *variable* II
    Here: extended „Moovac-I“ formulation (Oppermann et al., 2019)



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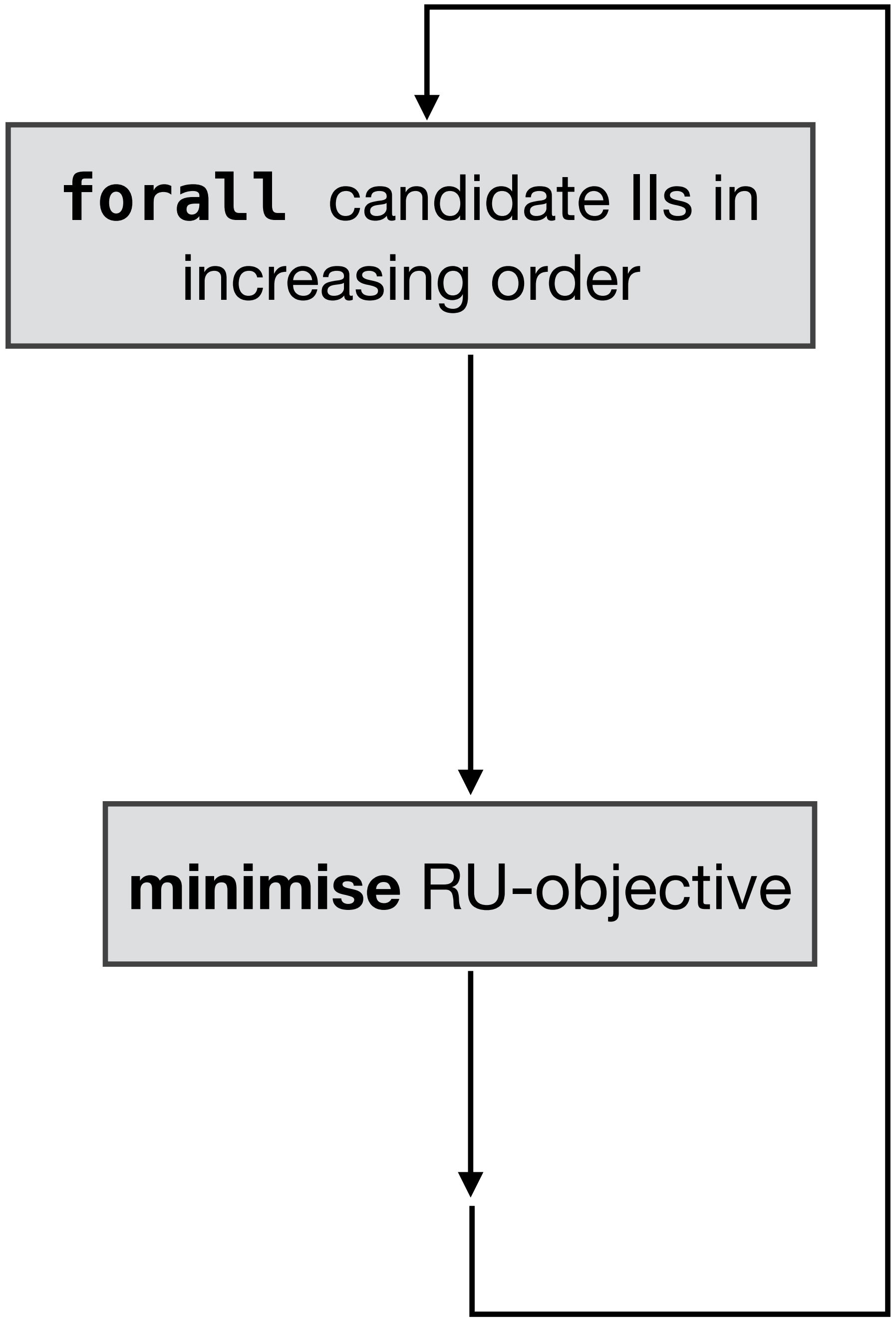

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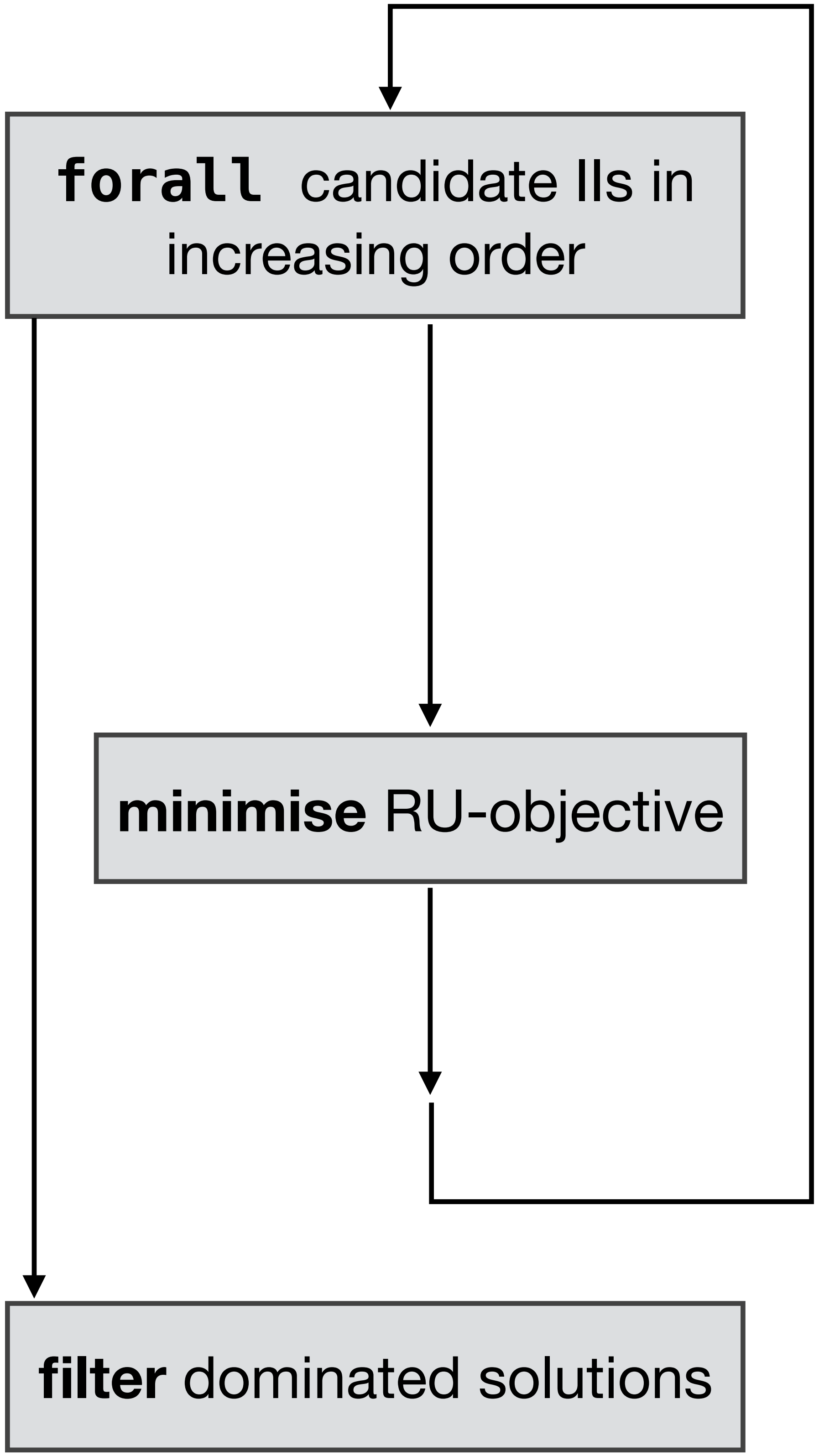
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Iterative Approach

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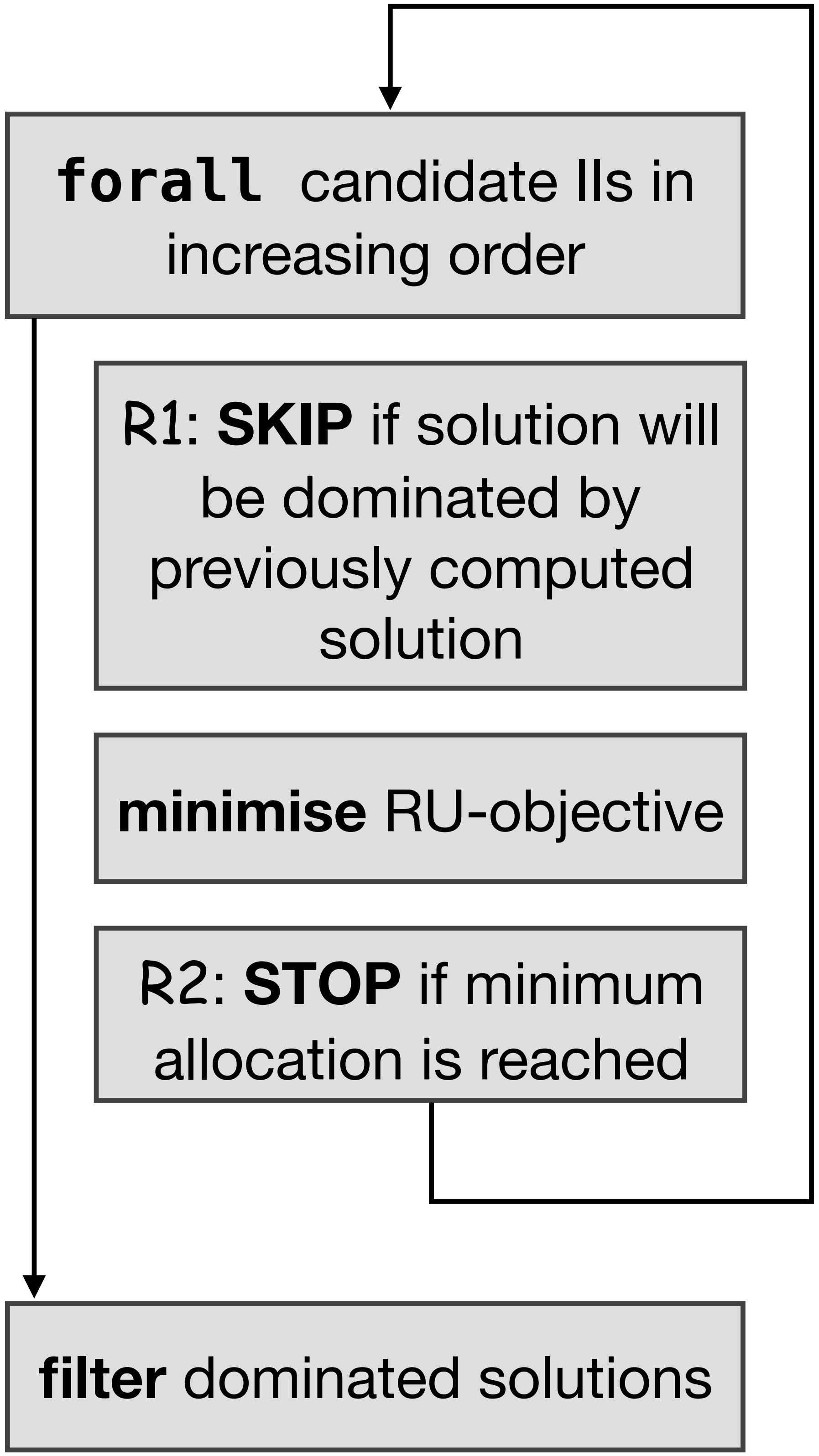
- We propose rules R1, R2 to compute fewer dominated solutions → next slide



forall candidate IIs in increasing order
R1: **SKIP** if solution will be dominated by previously computed solution
minimise RU-objective
R2: **STOP** if minimum allocation is reached
filter dominated solutions

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    $$a_q = 1 \quad q \in \hat{Q}$$

    is found

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- □ Introduction to high-level synthesis
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Setup

- **Gurobi 8.1, 8 threads, 16 GiB RAM, 6h time limit per instance** on Xeon E5-2680 v3 servers @ 2.8 GHz

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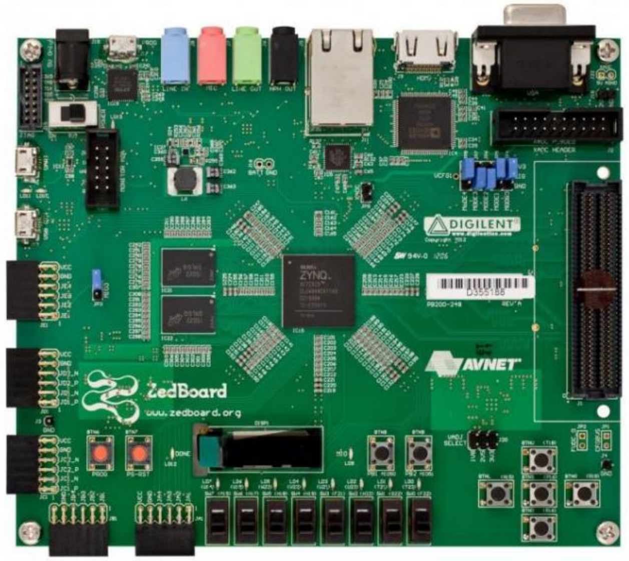

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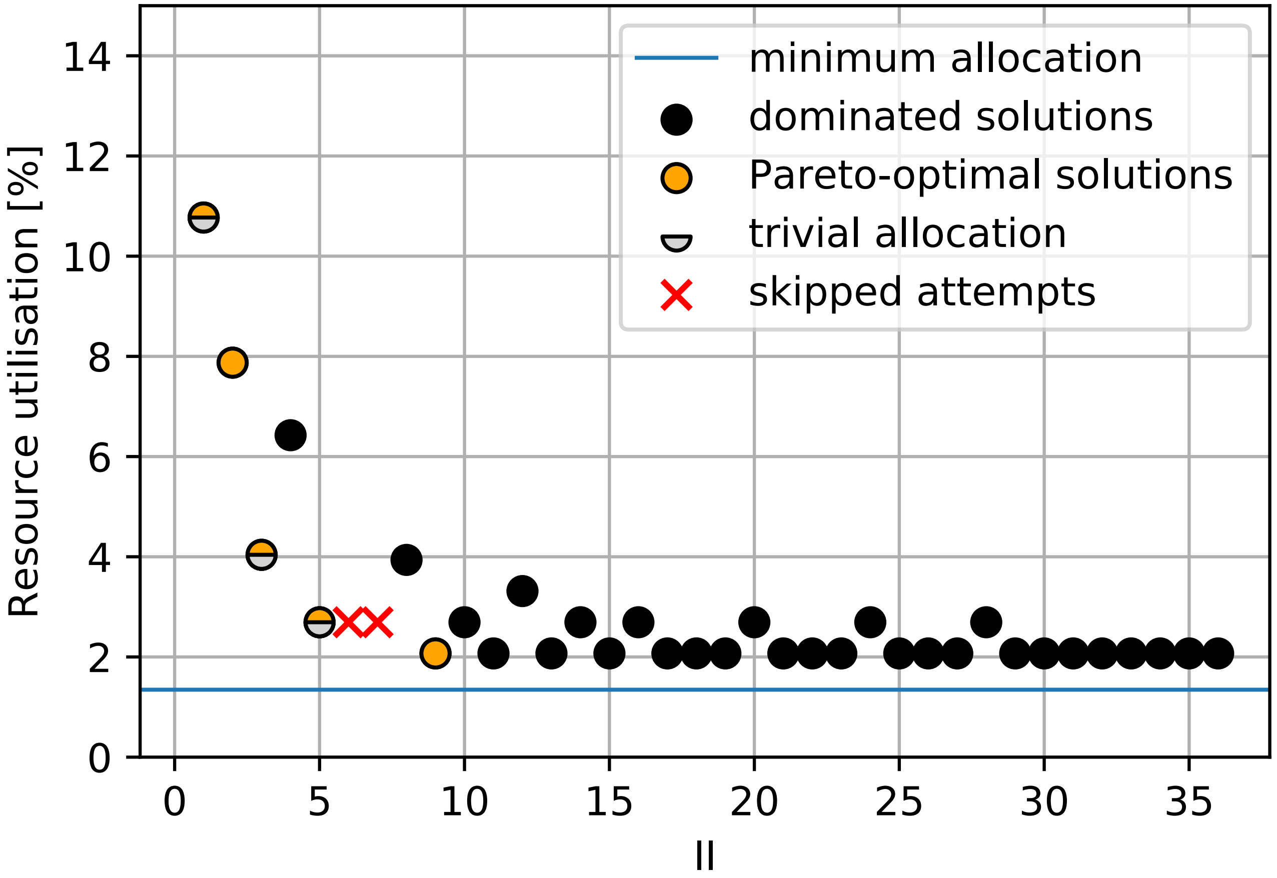

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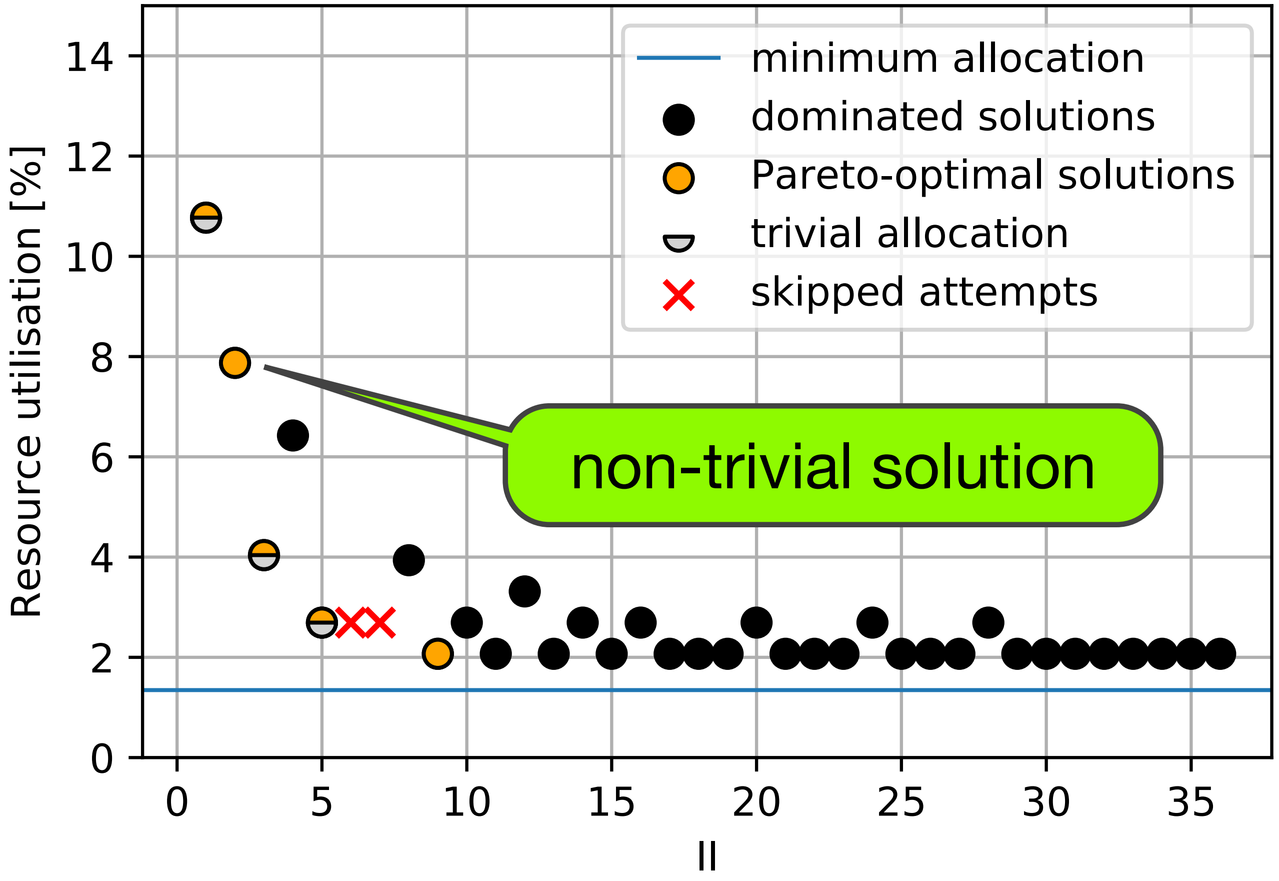

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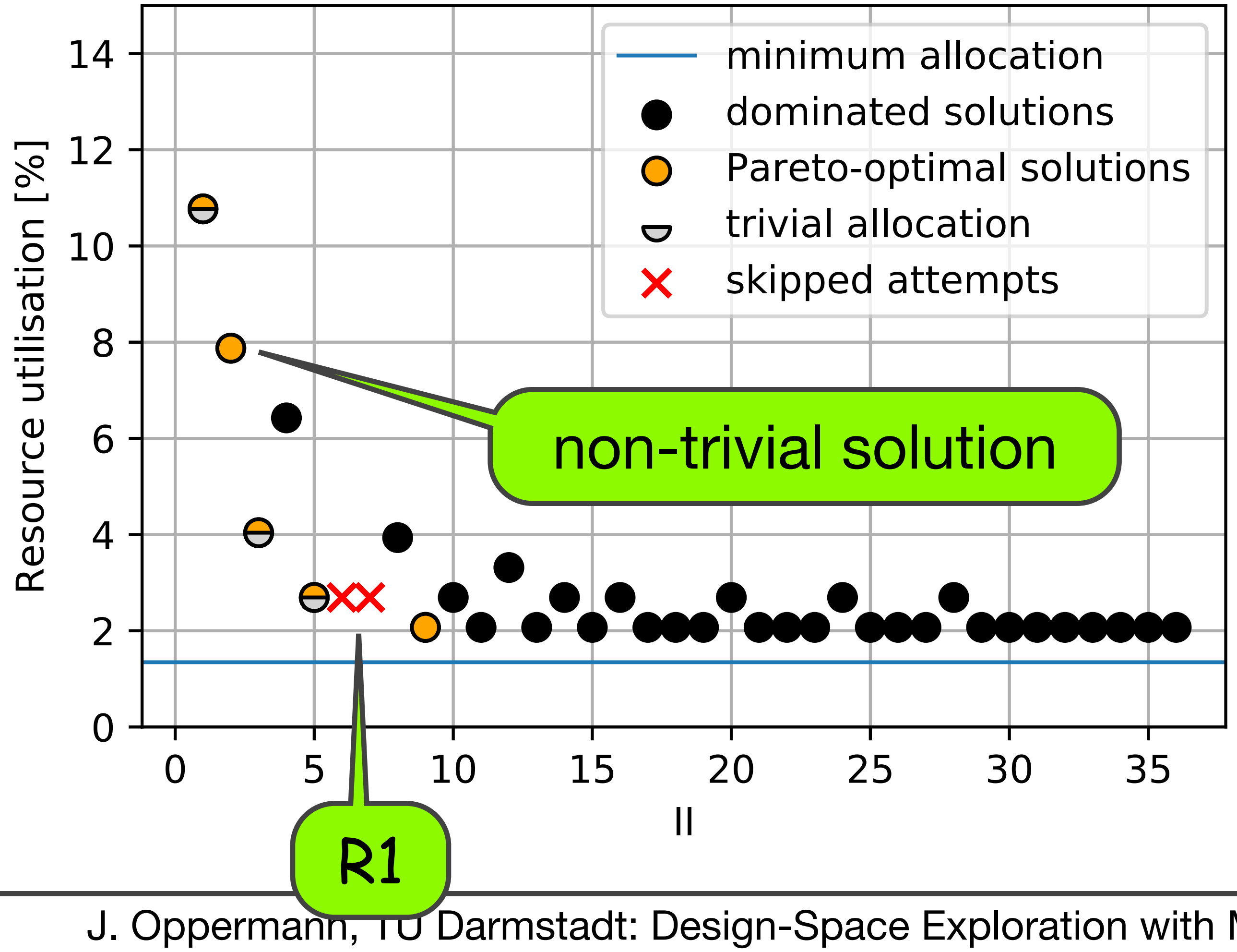

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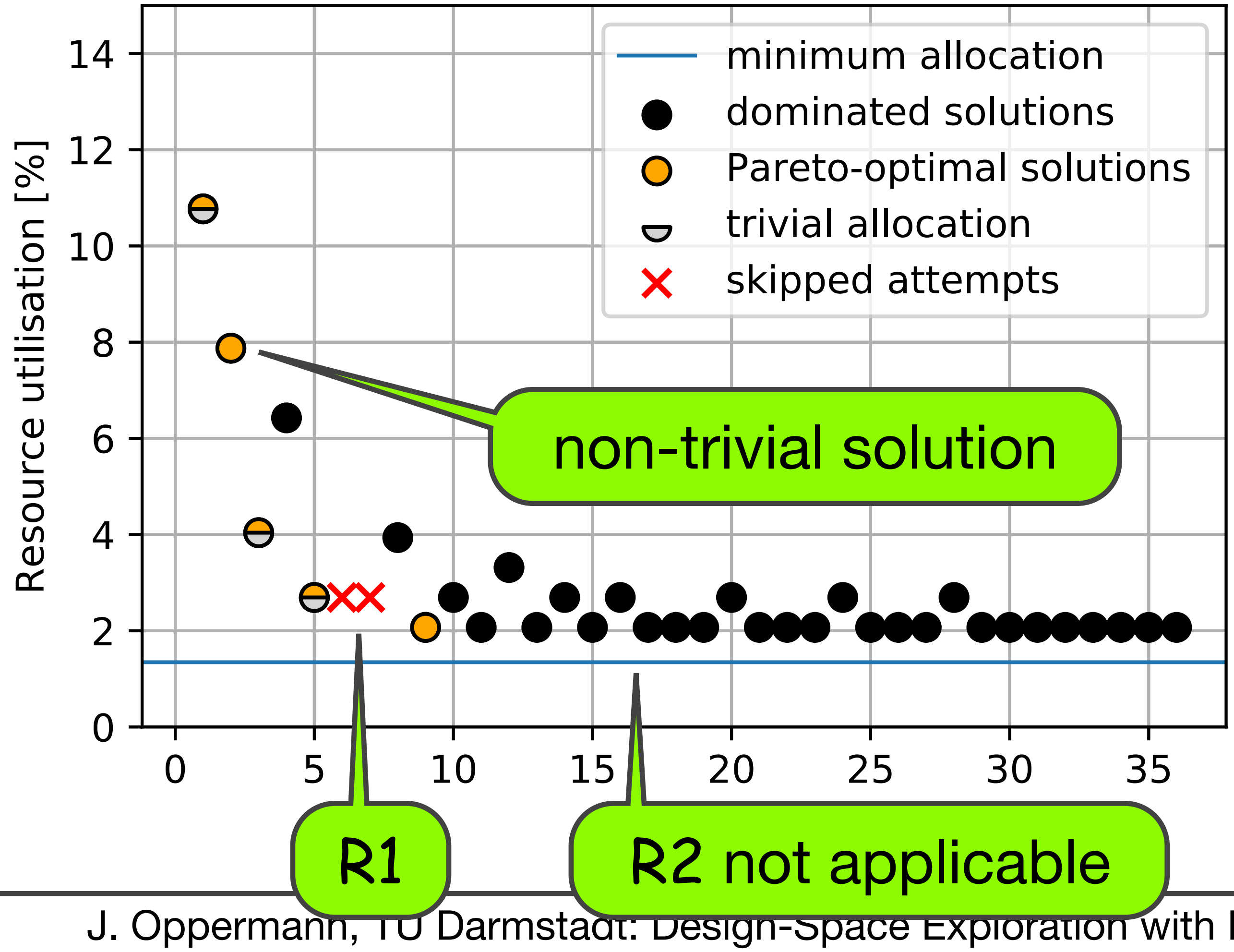

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R2 not applicable

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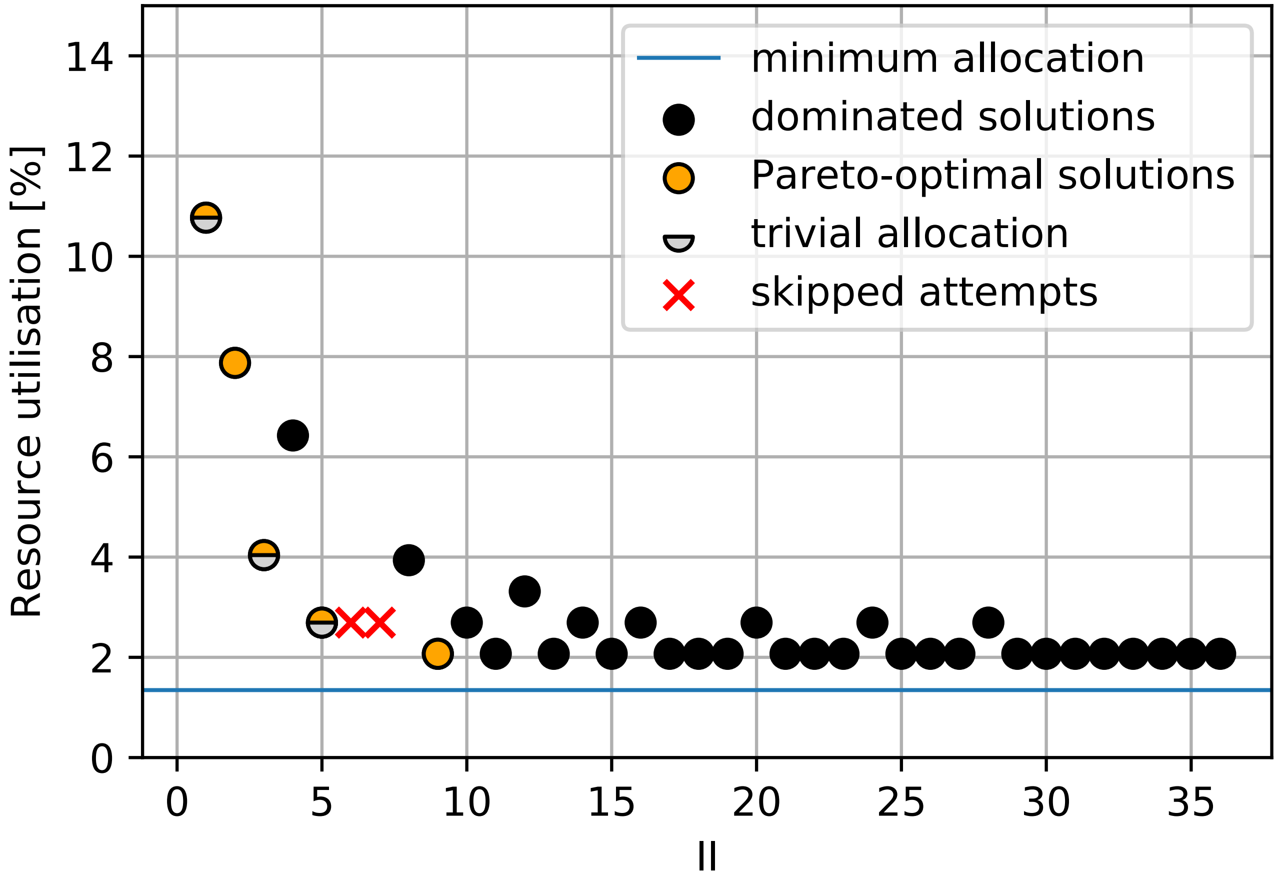
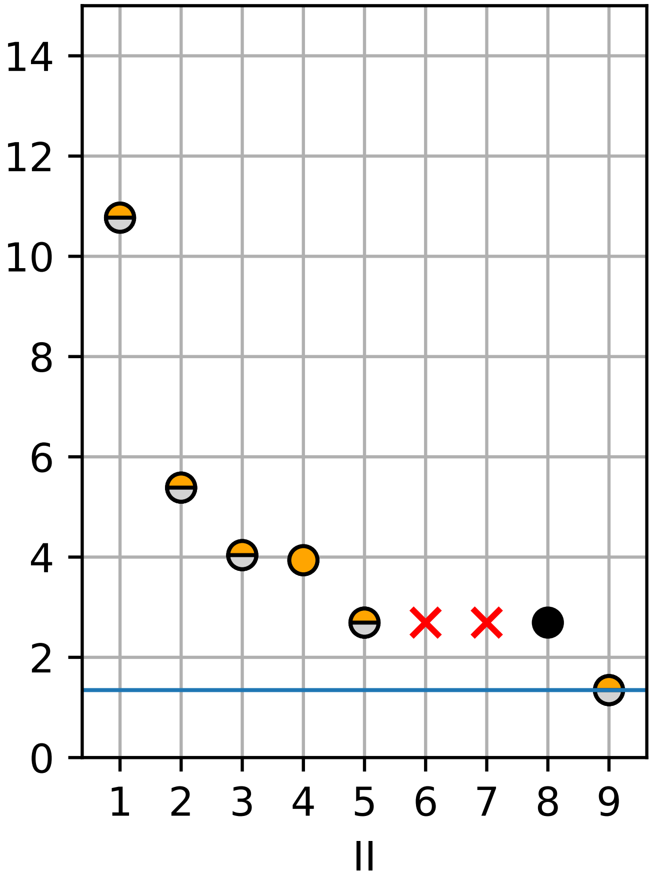


moderate = 37



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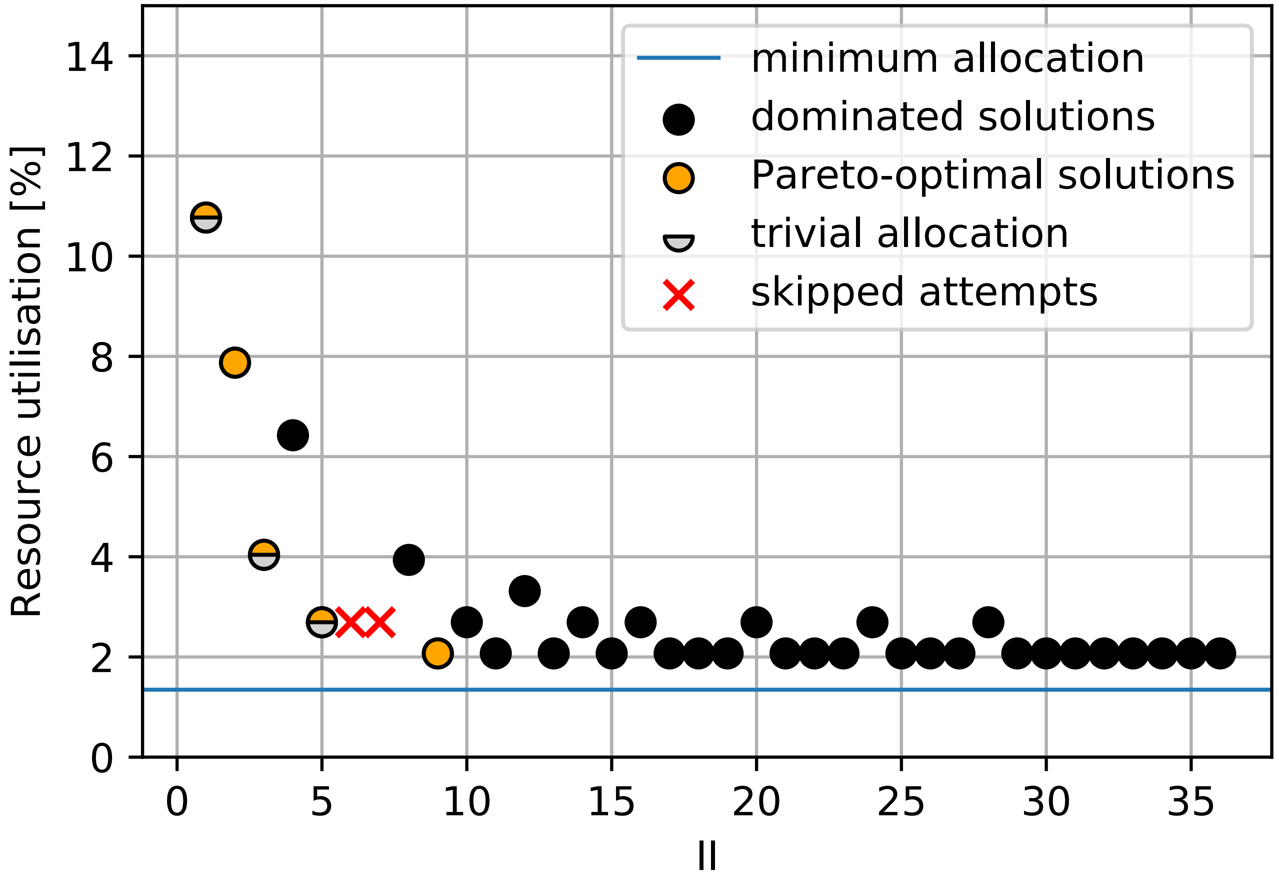

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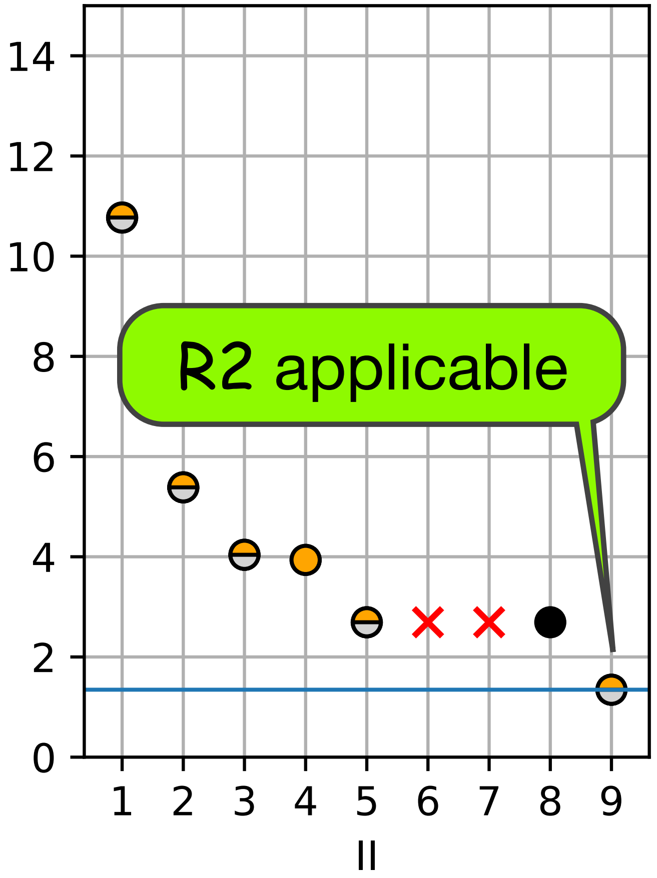

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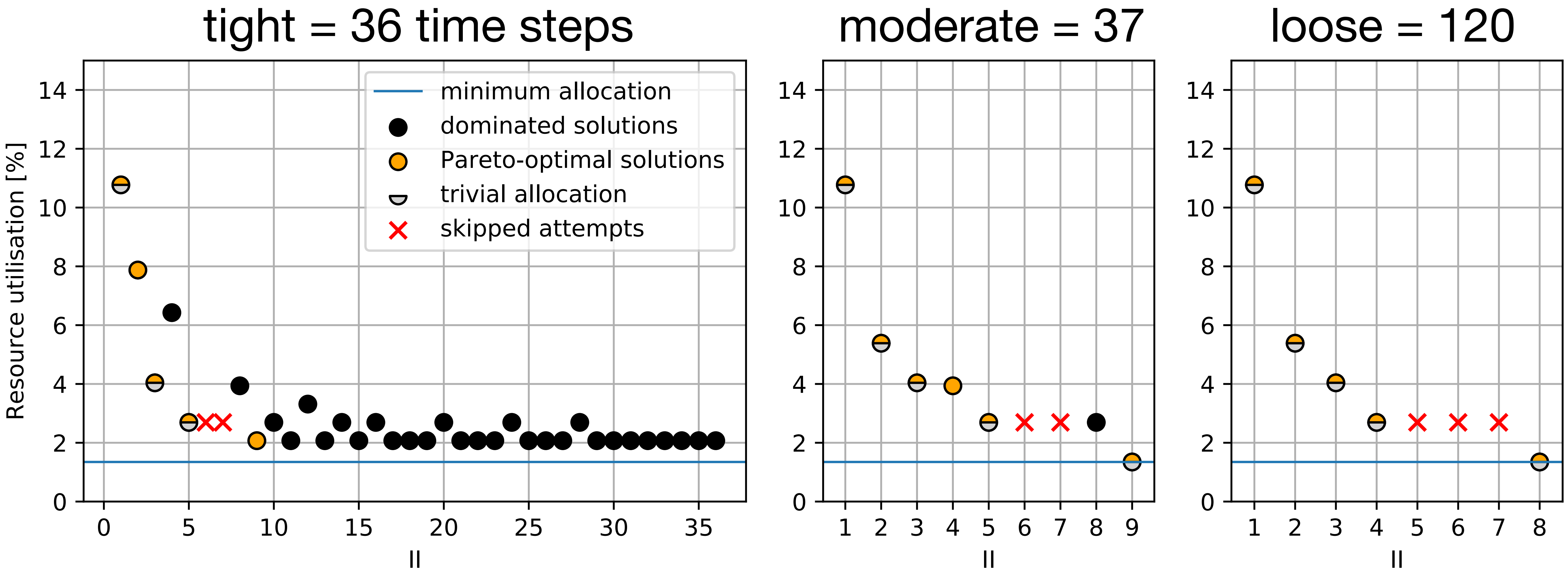

tight = 36 time steps

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loose = 120

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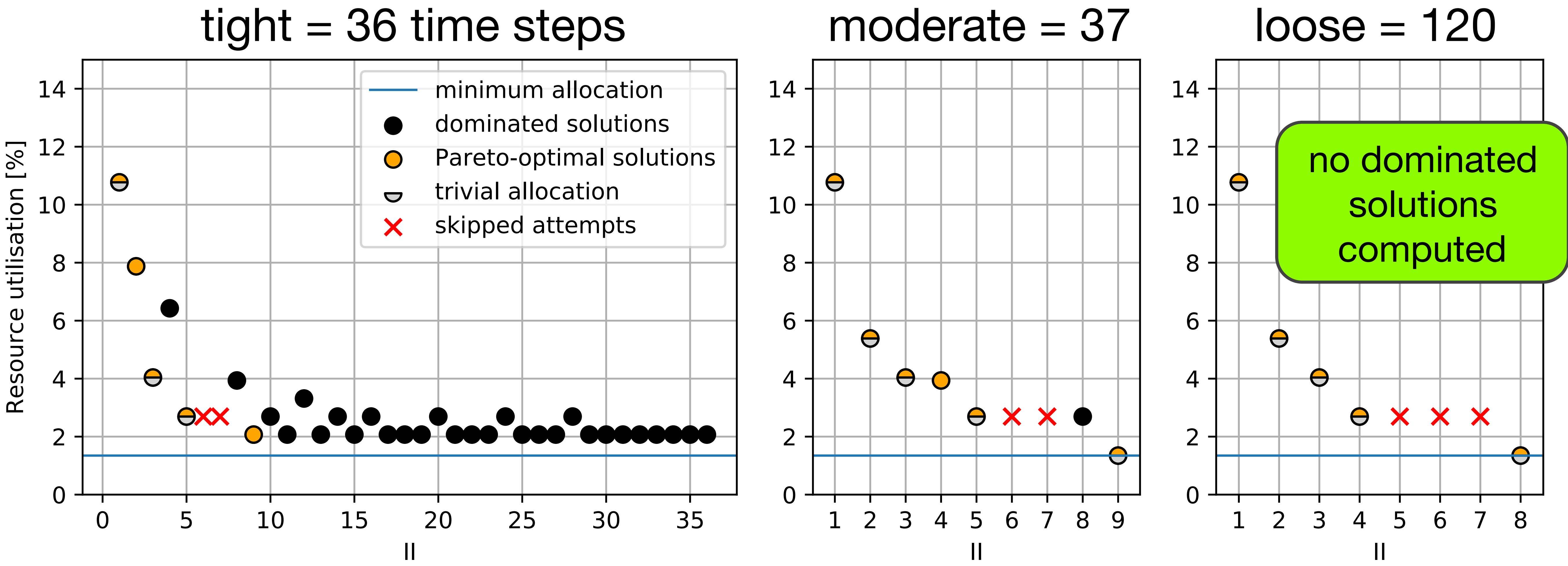
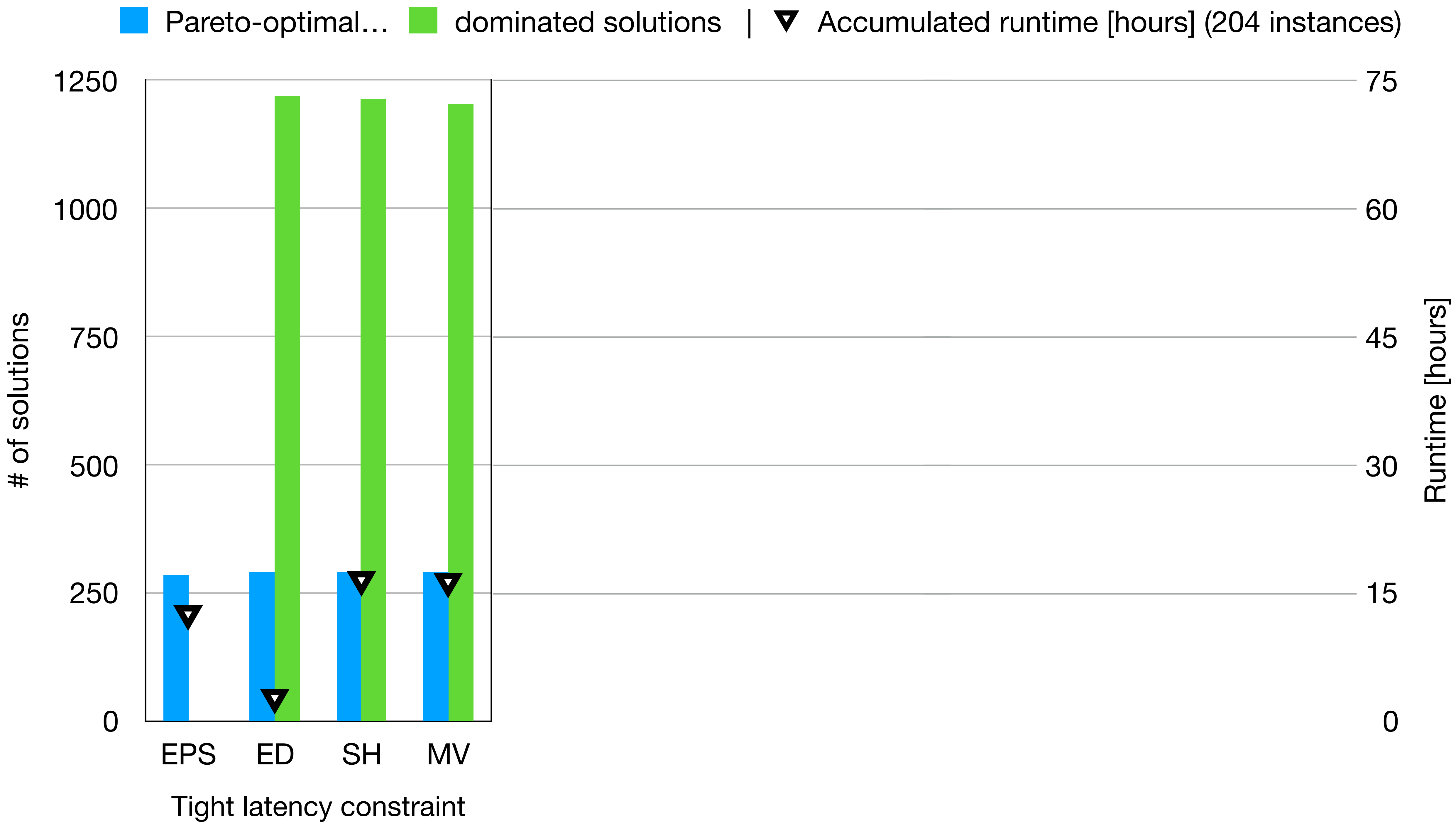


no dominated solutions computed

Scheduling Results

- Question: which approach computes the most Pareto-optimal solutions within 6 hours per instance?



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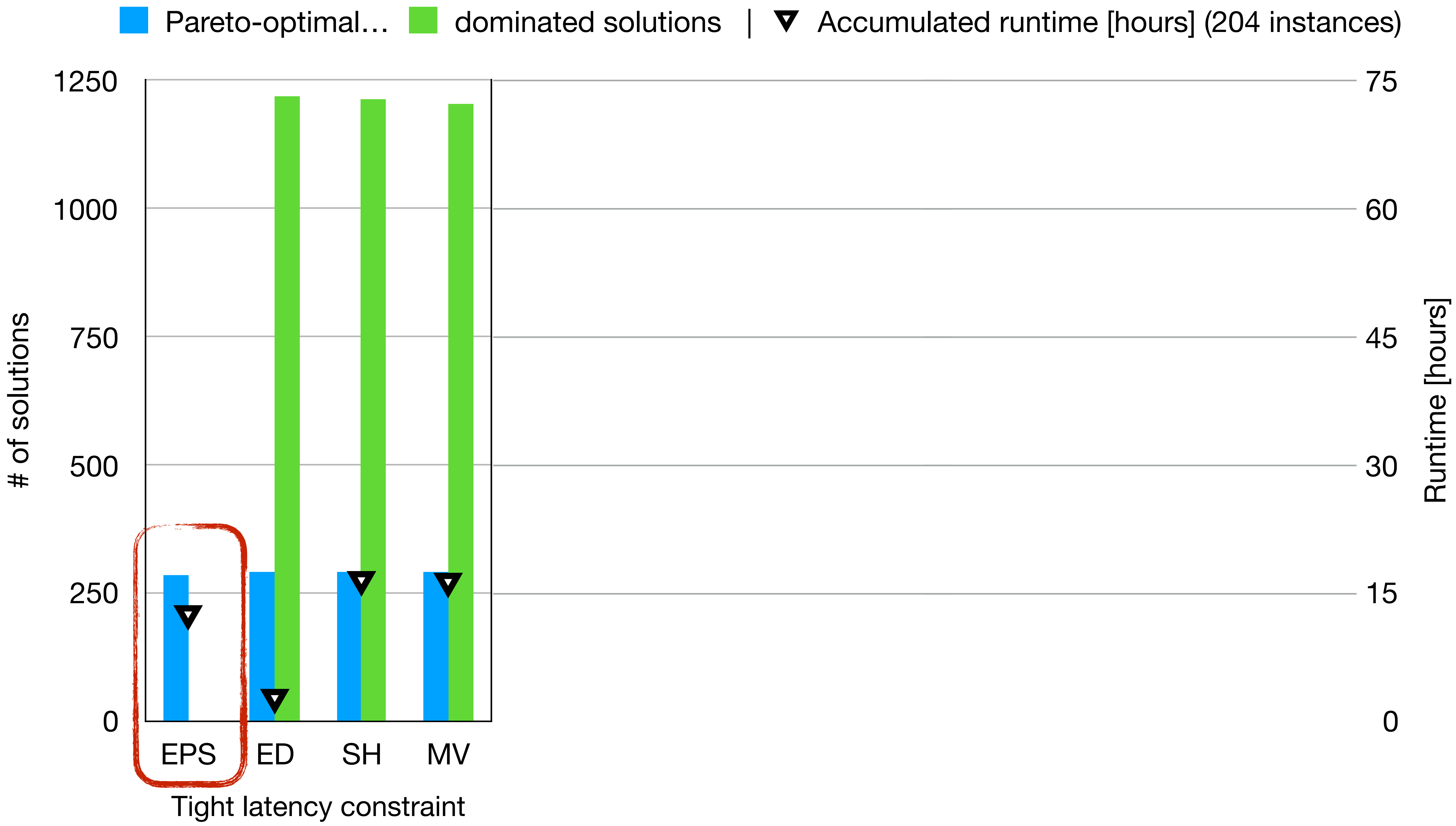

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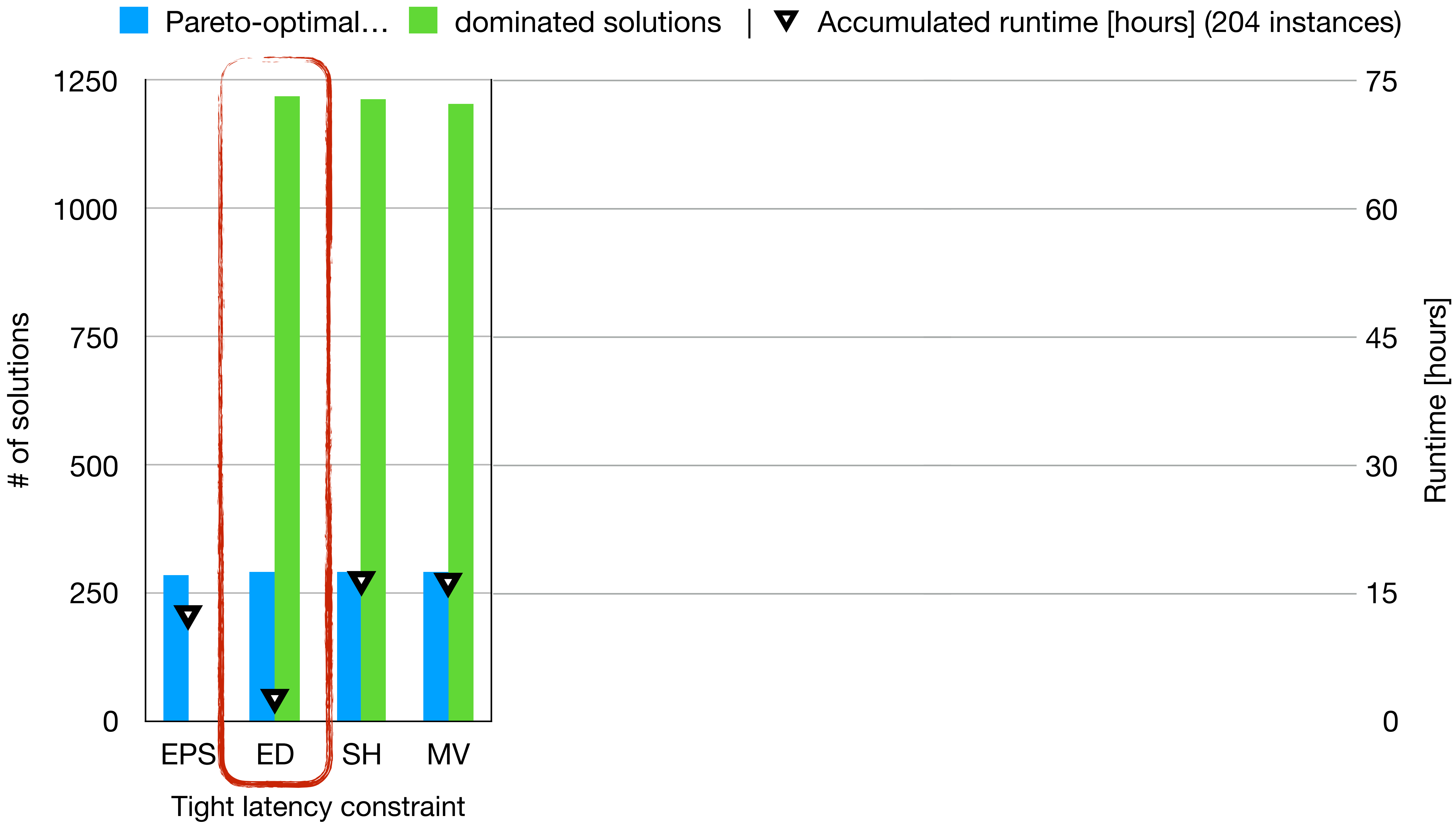

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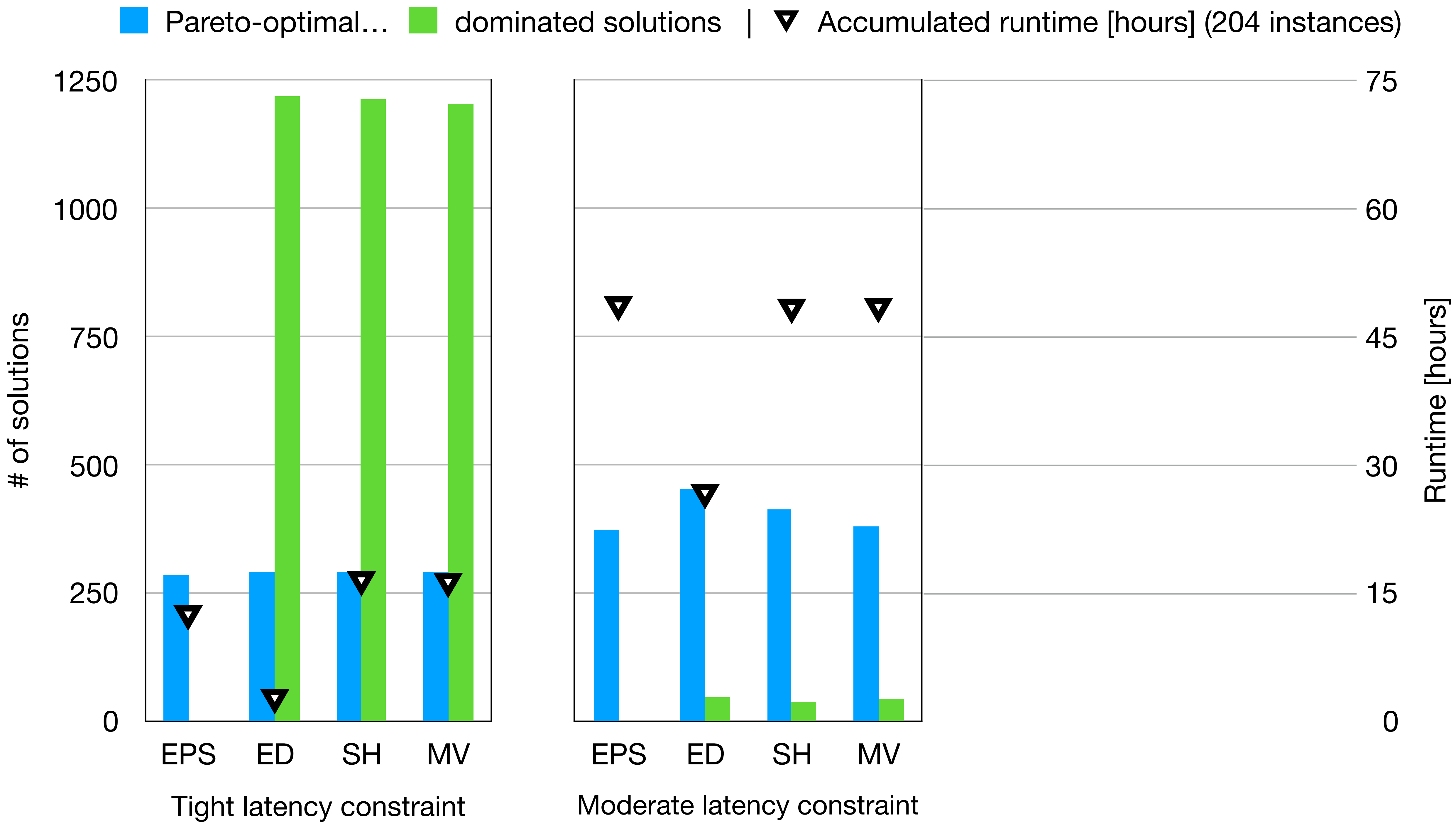

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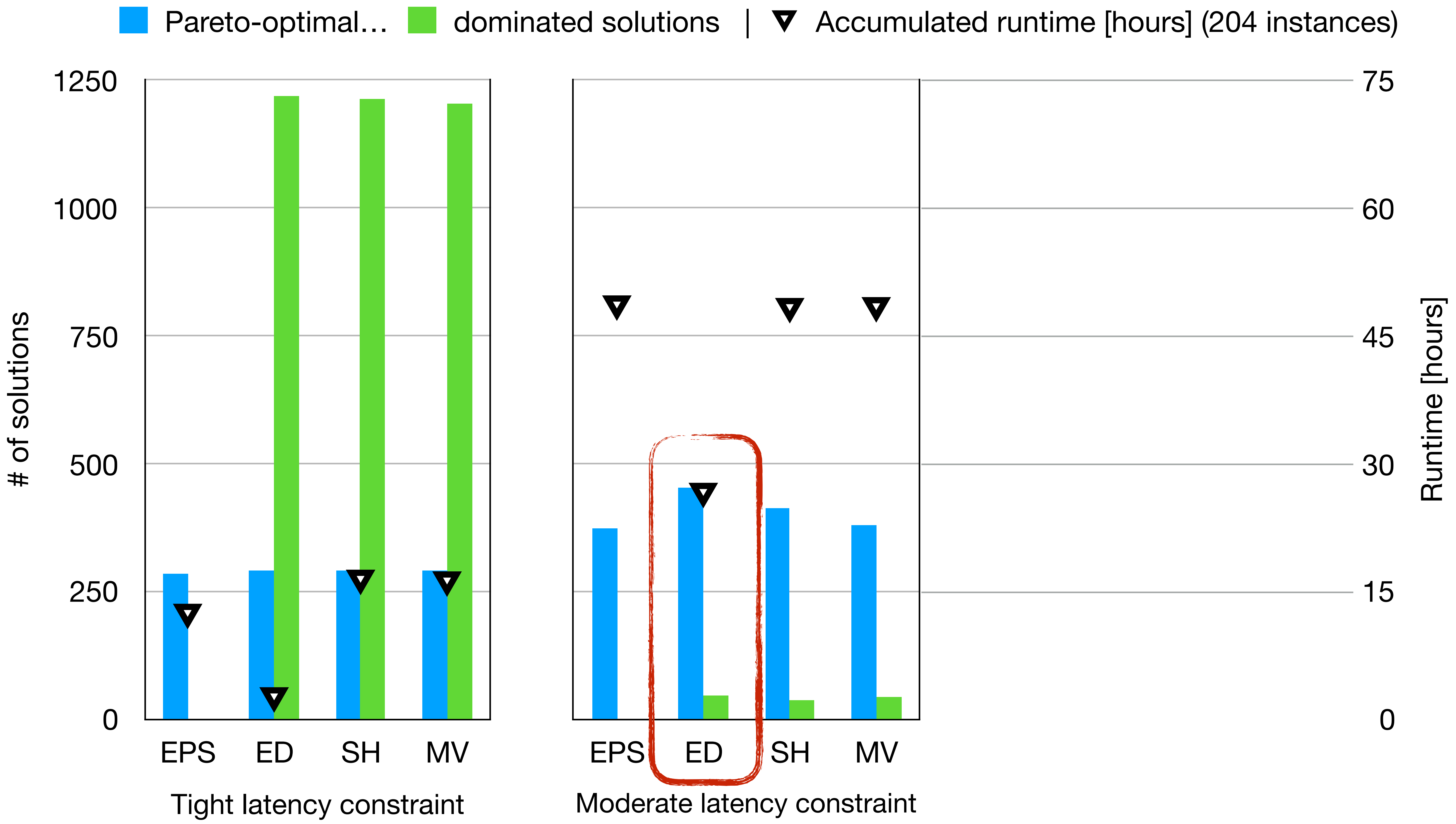

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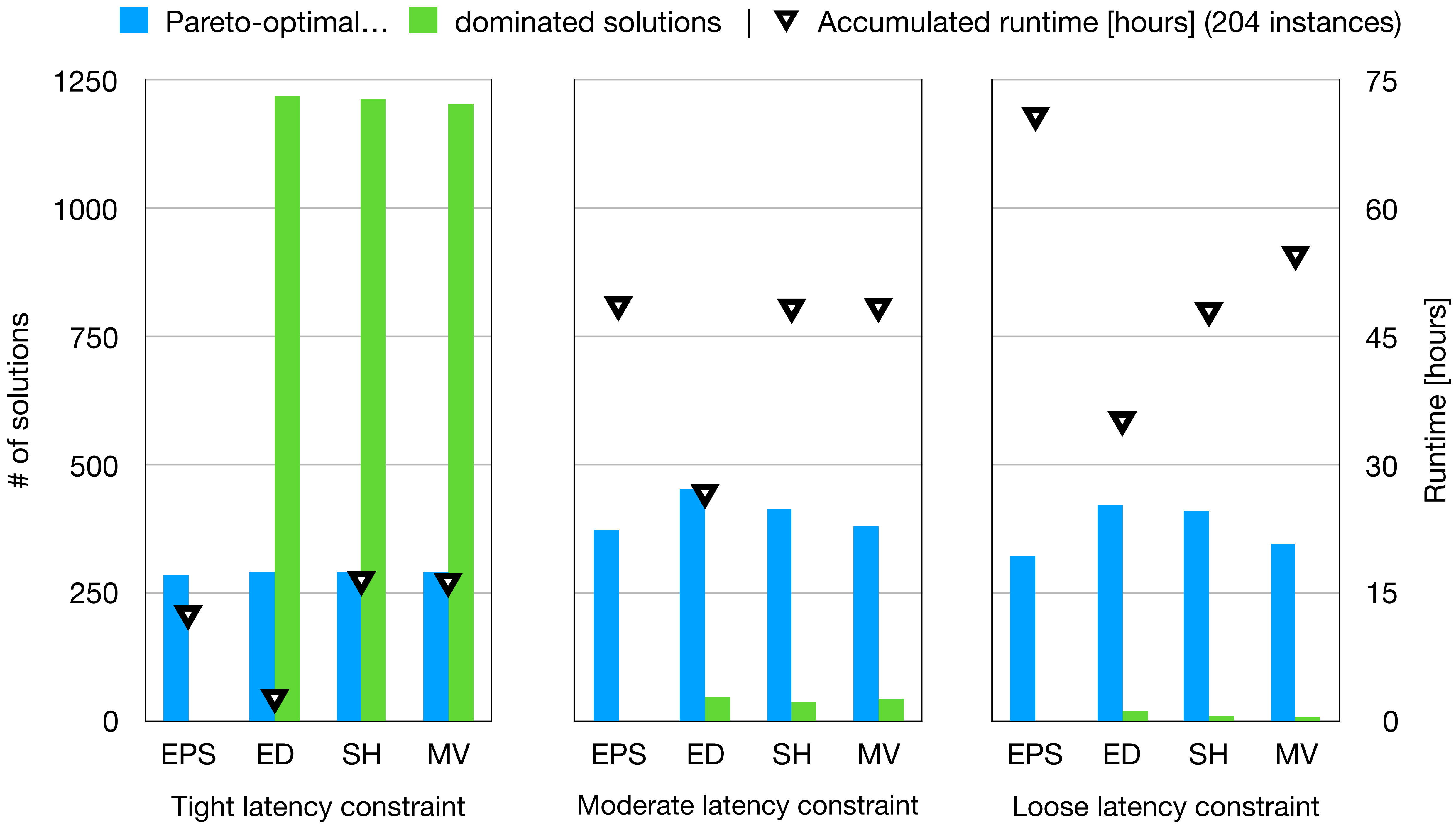

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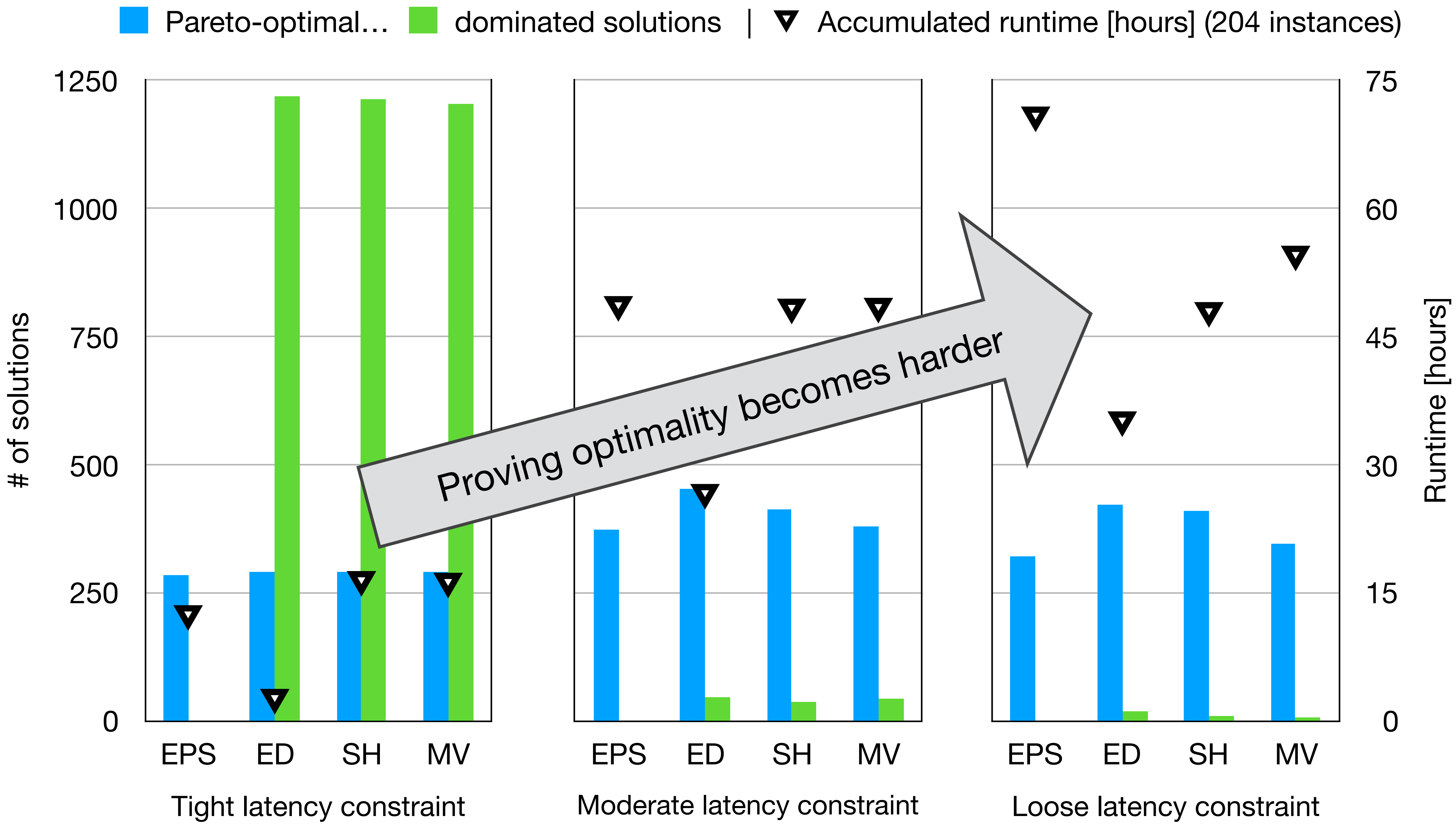

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- ED-formulation + iterative approach is fastest, and computes the most Pareto-optimal solutions
- Outlook: probably too many solutions per instance — how to determine relevant ones?

Thank you!

Check out the **HatScheT** scheduler library

http://uni-kassel.de/go/hatschet

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Hochschule Fulda
University of Applied Sciences

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Te Whare Wānanga o Tāmaki Makaurau
NEW ZEALAND

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KIT
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