Hardware-Accelerated Embedded Controller for a Piezo-electric Haptic Feedback System

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Abstract:
Piezo-electric ultrasonic actuators offer large static torque and precise rotary motion while avoiding self-motion when un-powered. In this work, a U164-11 ultrasonic piezo-electric module driving an Al_2O_3 ceramic ring is controlled by a Xilinx Spartan 6 FPGA to implement a haptic feedback system. The controller supports a runtime-adjustable capture detent resolution to enable the input of discrete values from varying domains. Furthermore, a hardware-accelerated speed control loop is implemented to compensate deviations of the motor speed caused by external forces. The control loop is executed in 12.5 ns and reduces the friction-induced fluctuations of the motor rotary-speed by 39 %.
Keywords: Piezo-electric motor, haptic feedback, reconfigurable logic, embedded system

Introduction

To operate a piezo-electric ultrasonic motor, the controller has to determine the current state-parameters of the actuator, e.g., the applied torque, the angle of rotation, or the angular speed. The current state has to be adjusted to user-provided target values by deriving actuating variables such as the amplitude and the frequency of the motor control signal as well as the desired rotation direction. In resonant operating mode, the frequency of the control signal is limited to a small band (about ±5 kHz) around the nominal value provided by the manufacturer. An initial calibration procedure can be used to find the optimal operating frequency influenced by ambient parameters such as temperature and pretention. However, the piezo-controller must be able to synthesize a periodic control signal of up to 160 kHz with a resolution of a few Hz. Here, digital frequency synthesis is preferable over analog frequency synthesis due to increased flexibility and accuracy as well as the smaller number of required components and the independency from ambient conditions [1].
To design an embedded controller for piezo-electric ultrasonic motors, a suitable computing unit has to be selected. Low power microcontrollers (MCUs) are typically not capable of synthesizing signals at the required frequencies. Digital Signal Processors (DSPs) are operated at higher frequencies and provide hardware-support for Multiply-Accumulate operations. However, even DSPs have to perform the data acquisition, the calculation of the actuating variables, and the digital frequency synthesis in a sequential manner. To overcome this sequential bottleneck, a Field Programmable Gate Array (FPGA) is used as the computing unit for the proposed embedded controller. FPGAs have been proven to be power-efficient alternatives to MCUs [2] and DSPs [3].
This work is organized as follows. After reviewing embedded and hardware-accelerated controllers for piezo-electric ultrasonic actuators, the design of the proposed actuator system and the implementation of two hardware-accelerated applications are detailed. Measurement results from the speed controller application are provided and discussed before concluding with an outlook to future work and practically relevant application scenarios.

Related Work

To evolve from laboratory test beds to practical applications, embedded controllers driving piezo-electric actuators are required.
Bekiroglu proposed an embedded controller for a traveling-wave ultrasonic motor (Shinsei USR60) based on an 8-bit MCU [4] [5]. An external circuit is used to synthesize the 42 kHz control signal. The actual motor speed, derived from counted encoder periods over 1 s, is adjusted to a target speed by stepping a reference voltage up or down. This reference voltage controls the external frequency synthesizer. As the actual frequency synthesis is performed externally and the control loop is executed just at 1 Hz, the computational requirements of this application are negligible.
Computationally more challenging controllers are based on reconfigurable logic. Jang et al. described a robotic arm driven by three ultrasonic motors (Shinsei USR60) [6]. Each motor is connected to an FPGA-based controller responsible for the acquisition of the motor status and the communication with a central controller. The central controller, also equipped with an FPGA, selects one of the motors at a time and applies the 42 kHz control signal. However, the frequency synthesis is performed by an additional integrated circuit and the proportional-integral control loop is calculated by an additional microcontroller. The authors did not justify the usage of additional hardware instead of

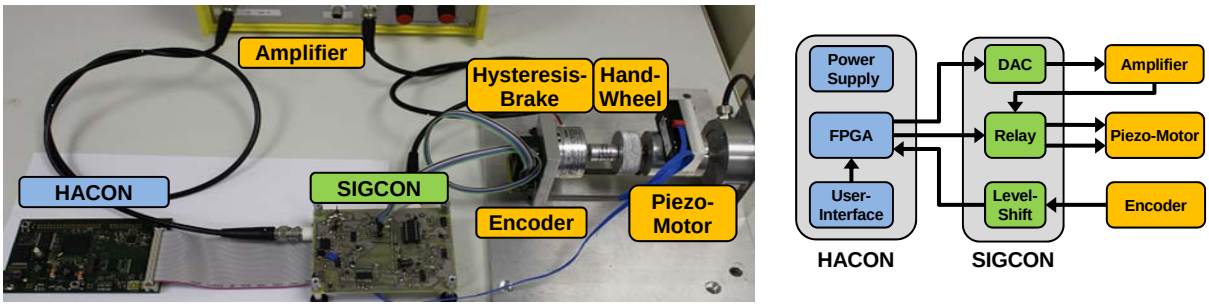

Figure 1: *Signal conditioning and processing in test bed*

utilizing the FPGAs also for signal synthesis and speed control.

Zhang et al. used an FPGA to synthesize four independent excitation signals up to 100 kHz to drive a multi-DOF ultrasonic motor [7]. Again, an additional DSP is employed for analyzing the encoder signals and calculating the control parameters (amplitude, frequency and phase shift), but without proper justification for using FPGA and DSP.

In contrast, Chen et al. [8] and Lin et al. [9] proposed embedded controllers mapping the whole signal processing chain to reconfigurable logic. The former utilized an Altera Complex Programmable Logic Device to calculate a speed control loop within 1 µs. The latter used a Xilinx Virtex 2 FPGA to implement a control law based on an Elman neural network to face nonlinear and time varying control conditions while driving a moving table by a piezo-electric ultrasonic motor.

In all applications described above, the piezo-elements are operated at about 40 kHz. In contrast, the piezo-motor used in the work at hand is driven at a frequency four times higher.

Actuator Design and Signal Processing Chain

The piezo-electric actuator used in this work is based on a U164-11 ultrasonic piezo-electric module by Physikinstrumente. It is encased and drives a Al_2O_3 ceramic ring with a diameter of 29 mm mounted on a steel shaft. A maximum output torque of 27 mNm and an idle speed of 176 rpm can be achieved while driving the actuator at 160 kHz and 130 V (peak to peak). An Avago Technologies HEDS-5600-A06 optical rotary encoder captures and feeds back the shaft angle with a resolution of 2000 steps per rotation. The actuator is integrated into a test stand equipped with a torque sensor (not used in this work), a hand wheel for manual rotation and a Mobac HB-10M-2DS hysteresis-brake for generating a speed independent resistive torque.

As shown in Figure 1, the embedded controller is implemented by two custom printed circuit boards (PCB): The first one, termed hardware accelerated controller (HACON), realizes the digital logic, using a Xilinx Spartan 6 FPGA device (XC6SLX150-3FGG484). Dedicated hardware modules control the external DAC, interpret the rotary encoder signals, and generate the amplitude modulated 160 kHz actuator control signal. The second PCB, termed signal conditioning (SIGCON), implements the digital to analog conversion, analog filtering and voltage level shifts. The output of the CA3338 DAC is amplified (26x) by an external LE 150/100 EBW amplifier by Piezomechanik. The amplified signal is passed through a relay controlled by the FPGA to select the direction of the rotation of the piezo-motor.

Hardware-Accelerated Piezo-Controllers

Two applications were implemented as FPGA-modules described in VHDL.

Figure 2 details the implementation of a haptic feedback system emulating virtual capture detents with a runtime-adjustable granularity. As soon as a user manually rotates the hand wheel, the encoder signals are interpreted to derive the current position φ and rotation direction. The detent granularity G is selected by a switch-addressed lookup-table and used to slice the motor position φ into regular

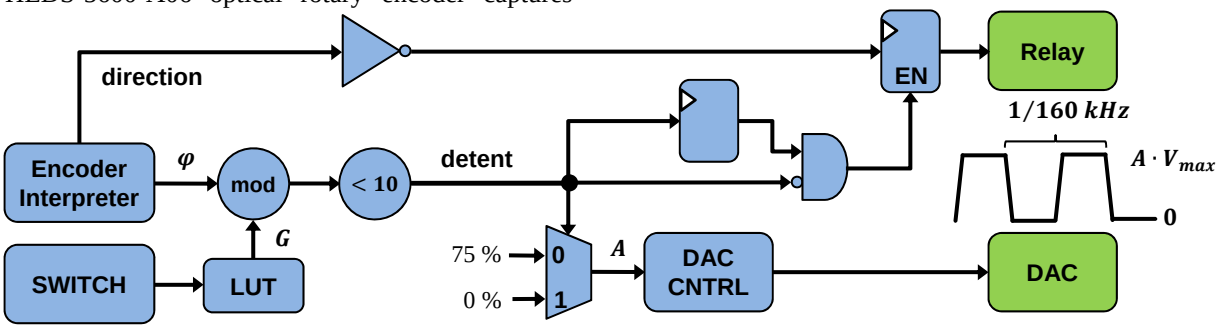

Figure 2: *Hardware-accelerated haptic feedback emulating virtual capture detents*

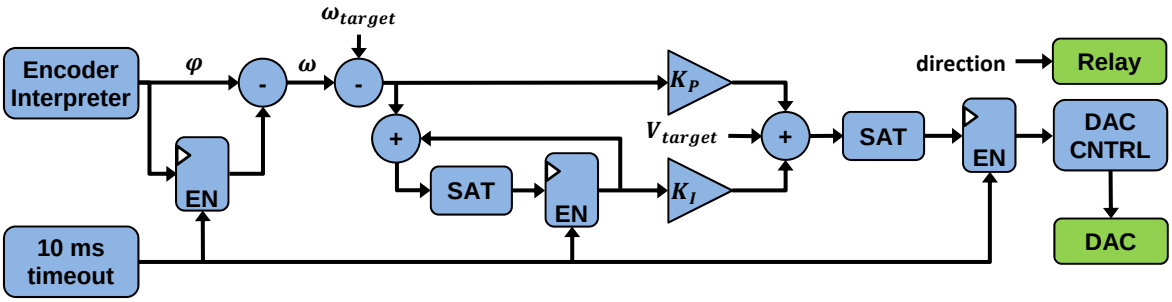

Figure 3: *Hardware-accelerated speed controller*

inter-detent sections. A threshold based detent-detection avoids the oscillation of the relay around the virtual detents. The inverse rotation direction is sampled on leaving a capture detent and applied to the relay to generate a counterforce against the manual rotation. Outside the detent position, the piezo-motor is driven by a 160 kHz square wave with a fixed amplitude. The generated resistive torque drives the system back into the last detent point. The amplitude is reduced to 75 % of the maximum possible value to avoid overshooting the detent position.

Figure 3 details the implementation of the hardware-accelerated proportional integral speed controller. Again, the encoder-interpreter derives the current position φ of the piezo-motor from the encoder signals. A motor speed-proportional variable $\omega(t) = \varphi(t) - \varphi(t - 10\,ms)$ is derived without actually dividing by the 10 ms averaging interval. Instead, all relevant application constants are multiplied by 10 ms at compile time. The deviation of the actual speed from a static target speed ω_{target} is calculated and accumulated over subsequent sampling cycles. The saturated accumulator serves as the integrative factor of the PI-controller. The additional static offset V_{target} amounts to the amplitude of the motor-control signal required to drive the unloaded piezo-motor at ω_{target}.

The final saturation of the actuating variable ensures a motor signal amplitude of at least 41.6 V to prevent abrupt halt of the motor caused by friction. Again, the DAC-controller generates a 160 kHz square wave with the calculated amplitude.

Evaluation Results

Figure 4 shows the characteristics of the motor speed at a fixed control signal amplitude of 78 V, corresponding to 3 V at the DAC output. The speed signal was derived by an offline analysis of the encoder signals. Prior to the activation of the hysteresis brake at $t = 0\,s$, the revolution oscillates around the mean value of 108 rpm with a dynamic range of 92 rpm. These fluctuations are caused by non-constant friction between the piezo-element's frictional contact and the ceramic ring. They are repeated with each rotation. After applying the external braking force, the average speed decreases to 80 rpm.

Figure 5 shows the results of the same experimental setup, this time with activated speed control loop. The initial fluctuations around the target speed are reduced to 56 rpm, i.e. 61 % of the unregulated case. After applying the external braking force, the average speed decreases to 89 rpm. The remaining control deviation is thus reduced by 32 %.

Both hardware-accelerated applications were combined into a single hardware-design sharing the encoder-interpreter and DAC-controller. These modules were described in VHDL, synthesized, and mapped using the Xilinx ISE 14.7 design automation tool. Less than 1 % of the FPGA logic resources are

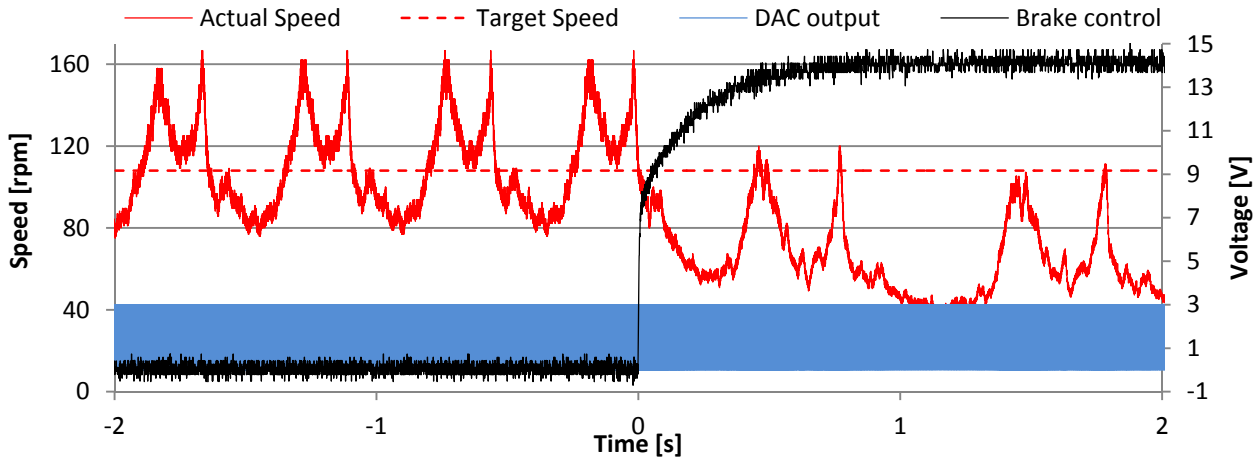

Figure 4: *Uncontrolled motor speed before and after activation of hysteresis brake*

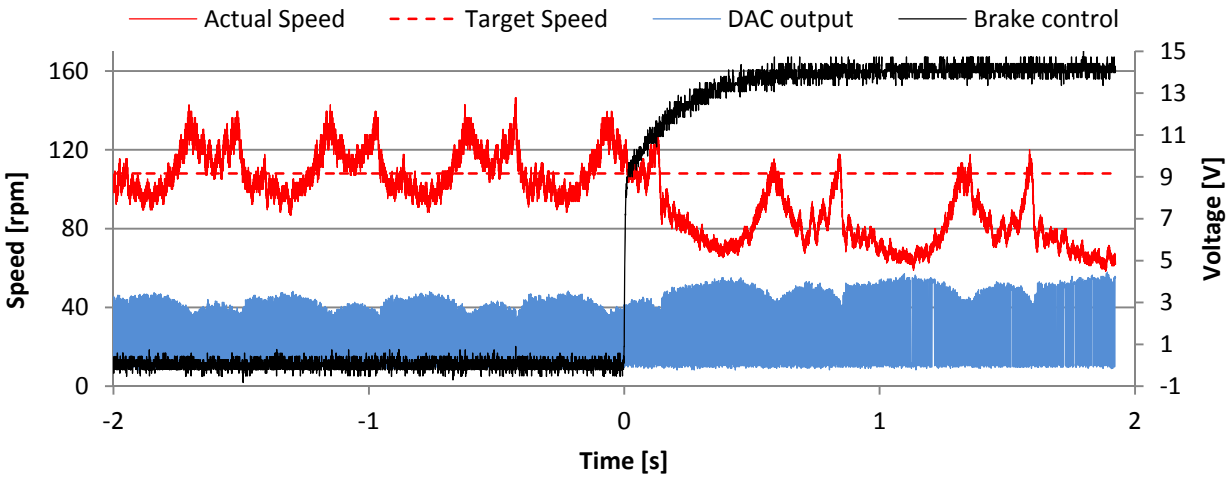

Figure 5: *Regulated motor speed before and after activation of hysteresis brake* $(\omega_{target} = 108\ \text{rpm},\ V_{target} = 3\ \text{V}, K_P = 4, K_I = 0)$

required for the described applications. The hardware modules may be operated at 80 MHz. As the PI-control-loop is executed in a single cycle, the controller processing delay (12.5 ns) is smaller than the period of the motor driving signal.

Conclusion

The proposed haptic feedback is clearly perceptible and allows for precise input of discrete values. It may be supplemented by a low frequency clattering to inform about critical or invalid inputs. Automotive infotainment systems are practical applications scenarios for this kind of user interface. The convolution controller reduces deviations of the motor speed from a given target value. The small utilization of the FPGA resources allows for using a smaller (cheaper) device or the implementation of more complex control rules, e.g., model predictive control.

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References

[1] M. Xuehua and W. Jinzhang, “Development of frequency synthesizer based on DDS+PLL,” in *Proceedings of the IEEE CIE Intern. Conference on Radar*, 2011.

[2] A. Engel, B. Liebig and A. Koch, “Energy-efficient heterogeneous reconfigurable sensor node for distributed structural health monitoring,” in *Conference on Design and Architectures for Signal and Image Processing (DASIP)*, Karlsruhe, 2012.

[3] A. Engel, B. Liebig and A. Koch, “Feasibility Analysis of Reconfigurable Computing in Low-Power Wireless Sensor Applications,” in *Reconfigurable Computing: Architectures, Tools and Applications*, Belfast, 2011.

[4] E. Bekiroglu, “Microcontroller-based full control of ultrasonic motor with frequency and voltage adjusting,” *Sensors and Actuators A: Physical*, pp. 151-159, 2008.

[5] E. Bekiroglu, “Ultrasonic motors: Their models, drives, controls and applications,” *Journal of Electroceramics*, pp. 277-286, April 2012.

[6] M. Jang, F. Dawson and G. Bailak, “Control system for multiple joint robotic arm powered by ultrasonic motor,” in *Proceedings of the 19th IEEE Applied Power Electronics Conference and Exposition*, 2004.

[7] M. Zhang, M. Li and L. Sun, “A Multi-DOF Ultrasonic Motor Using In-plane Deformation of PZT Elements and Its Driving Circuit,” in *Proccedings of the International Conference on Mechatronics and Automation*, 2007.

[8] J.-S. Chen and I.-D. Lin, “Toward the implementation of an ultrasonic motor servo drive using FPGA,” *Mechatronics*, pp. 511-524, May 2002.

[9] F.-J. Lin, Y.-C. Hung and S.-Y. Chen, “FPGA-Based Computed Force Control System Using Elman Neural Network for Linear Ultrasonic Motor,” *IEEE Transactions on Industrial Electronics*, pp. 1238-1253, April 2009.