

LLVM / MLIR dialect development

Student assistant position (all genders)

Embedded Systems and Applications Group



TECHNISCHE
UNIVERSITÄT
DARMSTADT

The free and open RISC-V instruction set architecture (ISA) aims to enable innovation in a traditionally very proprietary and closed field, and currently receives a lot of attention in academia, as well as growing industry support. As part of the Scale4Edge¹ project, the ESA group is developing a toolchain to integrate custom ISA extensions (ISAX), described in a high-level domain-specific language, CoreDSL², into RISC-V processor cores suitable for IoT settings.

Your **task** will be to help designing and implementing a custom dialect to represent a CoreDSL description in MLIR³. You will be defining new ops, writing canonicalisation and optimisation patterns, and implementing lowerings. Your work will become the entry point for the high-level synthesis system we develop for Scale4Edge.

Our **ideal candidate** is described by the following traits⁴:

- Passion for compiler engineering, and a very good understanding of intermediate representations, e.g. obtained from attending the Compiler II lecture.
- Ability to understand the Toy tutorial⁵. Actual prior experience with MLIR is of course a big plus.
- Familiarity with modern C++ development. Don't be afraid, MLIR is an excellent environment to learn about advanced aspects of C++ during the job.
- Familiarity with CMake-based software development and Git version control.

We **offer**:

- A great opportunity to gain experience in *the* state-of-the-art compiler framework, and to contribute to a major research project (RISC-V will be *everywhere* in the future)!
- Option to participate in publications, and to prepare for a potential follow-up Bachelor's or Master's thesis in the area of high-level synthesis.
- Flexible work hours and the option to work remotely.

The number of hours per week/month is negotiable. The wage paid is the standard TU Darmstadt wage for student assistants (10€/h before B.Sc., 11.75€/h after B.Sc.).

If all that **sounds interesting** to you, describe your motivation and prior experience with compiler hacking and send it to Julian Oppermann <oppermann@esa.tu-darmstadt.de>, together with a short CV and an up-to-date record of grades (TUCaN screenshot sufficient).

¹<https://www.edacentrum.de/scale4edge/>

²<https://github.com/Minres/CoreDSL/wiki/CoreDSL-2-programmer's-manual>

³<https://mlir.llvm.org>

⁴MLIR pun intended ;-)

⁵<https://mlir.llvm.org/docs/Tutorials/Toy/>